

Optimization of Nanoscale Thyristors on SOI for High-Performance High-Density Memories

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Introduction

A CMOS-based thyristor device known as a Thin Capacitively Coupled Thyristor (TCCT) (Fig.1) has been introduced as a novel switching device for high-density high-performance memory applications on SOI [1]. Using the characteristic bi-stable I-V curve and a gate-assisted turn-on/turn-off switching mechanism, a SRAM cell one-fourth the cell size of conventional 6T-SRAM was demonstrated in a 130nm SOI CMOS logic technology [2] and a novel capacitor-less DRAM cell with high speed access time was reported [3]. Stable device operation over a temperature range from 0°C to 125°C may pose a challenge for the operation of the thyristor-based memory cell because bipolar device characteristics are more dependent on temperature than MOSFET characteristics. For example, the forward breakover voltage (V_{fb}) of an un-optimized thyristor (Fig. 2) degrades with increasing temperature, which can result in loss of the data "0" state.

In this paper, methods for achieving a manufacturable TCCT on SOI with excellent thermal stability and fast switching speed are reported for the first time. A carrier lifetime adjustment process was implemented and indium was used as a p-type dopant. By using these methods, we demonstrate a TCCT device with stable forward breakover voltage (V_{fb}) at 125°C and bipolar gain with significantly improved temperature response. Finally, we achieved a worst-case switching speed of less than 2.1 ns measured from a 9Mb T-RAM test chip.

Device Fabrication

Thyristor-based memory cells were fabricated in a 130nm SOI CMOS logic technology. Three photo/implantation steps were added to define various regions of the TCCT, as shown in Fig. 3. No additional deposition or diffusion steps or modification of thermal processes are required for TCCT device fabrication.

Modulating Temperature Dependence of NPN Gain

The gain of bipolar transistors increases with temperature. In this work, indium is employed as the p-base dopant species in order to modulate the temperature coefficient of NPN gain and stabilize thyristor characteristics over a wide operating temperature range. The base of an NPN bipolar transistor is typically doped with boron, which is nearly fully ionized over the operating temperature range of most semiconductor devices. Indium is known to have an acceptor level which is 156 meV above the top of the valence band of silicon. As a result, the fraction of ionized indium atoms increases with temperature, resulting in increased Gummel number and reduced gain.

Fig. 4 shows the measured data confirming that the temperature dependence of the NPN DC gain (β) has been modulated and even inverted by replacing boron with indium as the p-base dopant species.

Carrier Lifetime Adjustment with Nanoscale Uniformity

The forward-blocking capability of thyristors at high temperature can be improved by adding a shunt resistor to either or both base-emitter junctions. Although this technique has been effectively used in power applications, it is difficult to apply controllably to nanoscale thyristors for memory applications. In this paper, we introduce a carrier lifetime adjustment (leakage) implant at the anode/n-base (J1) junction for improving thermal stability. The principle of the leakage implant is similar to that used for source junctions of SOI MOSFET devices to suppress the floating body effect.

In SOI MOSFETs, the leakage implantation is typically applied at the S/D implantation step followed by the S/D RTA process. Fig. 5(a) shows the measured diode I-V curve for a 180nm-wide device from this process. The forward current of some devices at low-bias exhibits increased leakage due to the leakage implantation, but large device-to-device non-uniformity of the low-bias leakage characteristics is observed. The same leakage implantation was performed after the S/D RTA step and before the silicidation step (anneals less than 800°C). In this case, forward current uniformity is dramatically improved, as seen in Fig. 5(b). The uniformity of current for narrow devices is significantly improved by using low temperature annealing (implant after S/D RTA) as opposed to high temperature annealing (implant before S/D RTA).

Fig. 6 shows a series of XTEM images of the damage profile in silicon as-implanted and followed by various anneal conditions. It was observed that the defect size was small after low temperature annealing, but the size gradually increased with increasing annealing temperature. For nanoscale memory applications, low temperature annealing is desirable in order to achieve atomic-scale defects and therefore good uniformity in narrow-width devices. Such a low temperature annealing process is commonly used at the silicidation step in the conventional CMOS process. Fig. 7 shows measured J1 leakage current for various leakage implant conditions. By changing the implant conditions, modulation of leakage current (carrier lifetime) over two orders of magnitude is shown while maintaining good uniformity. Fig. 8 shows that good V_{fb} distribution at 125°C has been successfully achieved by carrier lifetime adjustment implant with low temperature annealing.

The switching speed of the TCCT device is determined by various device parameters such as npn and pnp bipolar gains, gate-to-pbase capacitive coupling ratio, and carrier lifetime τ in J1. Due to the unique gate coupling mechanism, the excess carriers in the p-base are removed at the falling edge of the gate pulse without carrier recombination; however, carriers in the n-base need to be removed by recombination. Therefore, the carrier lifetime in the J1 junction becomes a limiting factor for the turn-off switching speed. When τ is reduced, carriers in the n-base are more quickly recombined, resulting in improved turn-off speed. Fig. 9 shows the distribution of time required to write data "0" measured from a 9Mb T-RAM test chip at 125°C. A T-RAM cell with write time of less than 2.1ns is achieved for the slowest bit out of 9Mb. This array result confirms the good thermal stability of the TCCT device and successful control of carrier lifetime adjustment for all TCCT devices in large arrays.

Conclusion

This paper demonstrates a thermally stable TCCT device on SOI using carrier lifetime adjustment implantation and low temperature annealing. In addition, temperature sensitivity of bipolar gain is optimized using indium as a p-type dopant. Finally, write time less than 2.1ns is obtained from a 9Mb T-RAM test chip at 125°C. These results demonstrate that the TCCT device is a good candidate for highly reliable, high-density high-speed memory applications.

References

- [1] F. Nemati et al., 1999 IEDM Tech. Dig., pp. 283.
- [2] F. Nemati et al., 2004 IEDM Tech. Dig., pp. 273.
- [3] H.-J. Cho et al., 2005 IEDM Tech. Dig., pp. 321.

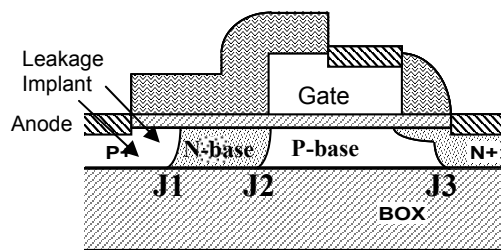


Figure 1: Schematic cross-section of a TCCT, showing junctions J1, J2, J3 and the application of an implant to reduce minority carrier lifetime in J1.

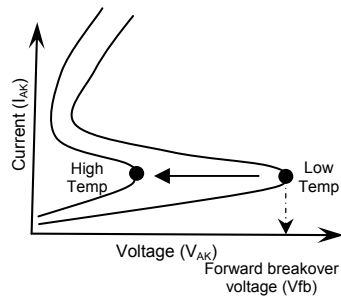


Figure 2: Thyristor I-V curves at low and high temperature before optimization.

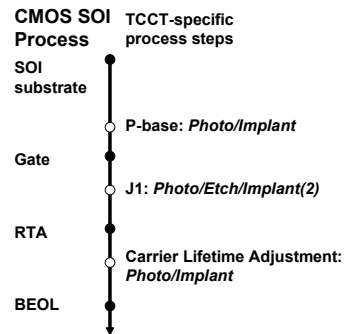


Figure 3: Process flow highlighting TCCT-specific steps.

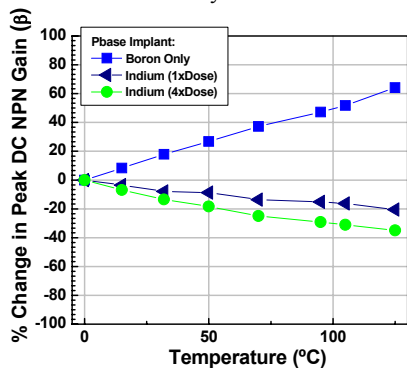


Figure 4: Measured peak NPN DC gain vs. temperature for various pbase implant species.

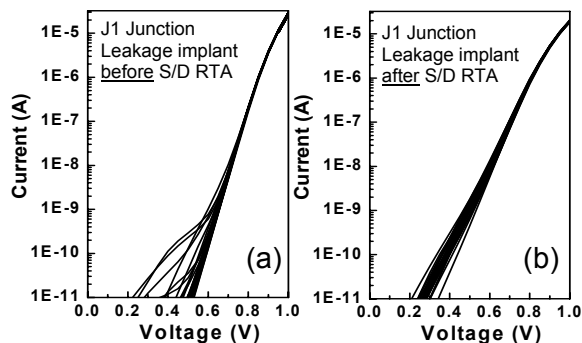


Figure 5: Measured J1 diode (PNP base-emitter junction) characteristics with leakage implant *after* S/D RTA show reduced variation. Active width is 180nm.

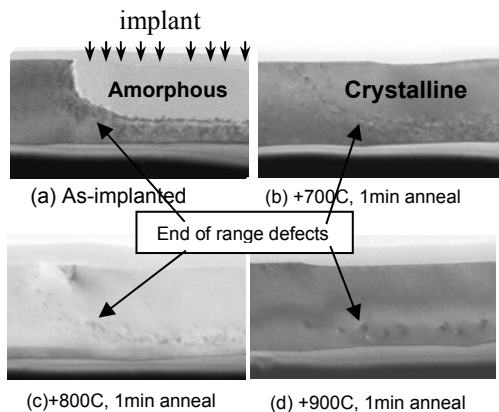


Figure 6: TEM images of J1 region. Higher temperature anneal results in fewer, larger defects.

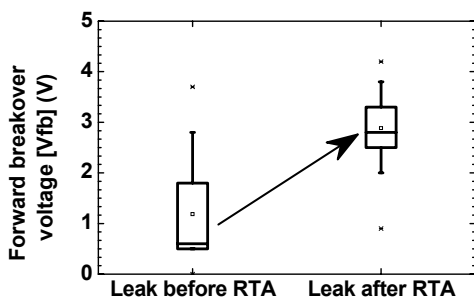


Figure 8: Measured forward breakover voltage distribution at 125°C shows improvement with leakage implant *after* S/D RTA.

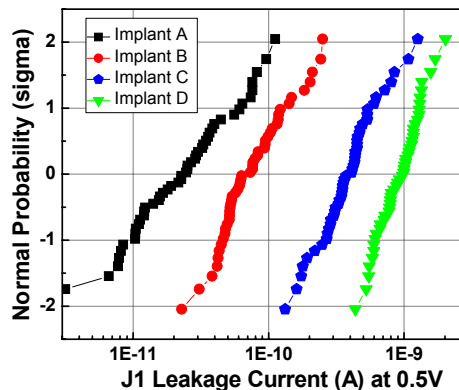


Figure 7: Measured distribution of narrow width (180nm) J1 junction leakage formed with leakage implant *after* S/D RTA.

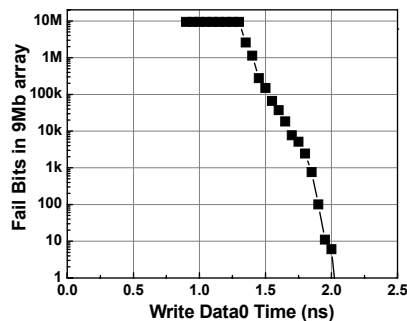


Figure 9: Measured distribution of time required to write data "0" in 9Mb test vehicle with optimized TCCT at 125°C.