Optimization of Substrate Doping for Back-Gate Control in SOI T-RAM Memory Technology

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Abstract

This paper presents various considerations for substrate doping optimization in SOI T-RAM technology. Back gate (substrate voltage) control is used in an SOI T-RAM technology for optimizing cell characteristics. However, it is reported for the first time that typical low-doped substrates used in SOI logic technologies can create unusually slow transient effects in T-RAM cell. It is also demonstrated that the optimization of substrate doping resolves this slow transient problem and improves back gate control of SOI T-RAM memory arrays.

Introduction

T-RAM (Thyristor-based Random Access Memory) is a novel memory cell technology that breaks through the performance-density limitations imposed by conventional memory cell technologies such as 6T-SRAM and DRAM, by providing SRAM-like performance at $1/4^{th}$ the cell area. T-RAM cell consists of a thin capacitively coupled thyristor (TCCT) and an NMOS access transistor (Figs.1,2). The memory effect in a T-RAM cell is based on the bistable S-type I-V characteristic of a thyristor (Fig.3), allowing a wide read margin, high read current, and a non-destructive read. The high-speed switching of TCCT, enabled by pulsing WL2 gate, provides a fast write speed. These features enable functionality and speed equal to 6T-SRAM. A T-RAM 9Mb memory array (Fig.4) has been previously demonstrated in a 130nm PD-SOI CMOS logic technology, simply integrated by adding photo-masks and implantation steps. XTEM image of T-RAM cell is shown in Fig.5. The cell size is 0.562 μm^2 (0.36 μm x 1.56 μm). A detailed description of this 130nm SOI T-RAM technology can be found in Ref. [1].

Back-gate control of T-RAM cell

The optimization of the gains of NPN and PNP bipolar devices constituting a TCCT can significantly improve cell stability. Controlling the voltage applied to the back substrate is an effective method for controlling and optimizing the NPN bipolar gain in a T-RAM cell without any adverse impact on MOSFETs. Voltage applied to the substrate induces an electric field in the BOX, which modulates the hole concentration in the p-base, the base Gummel number, and the NPN gain (Fig.6). Fig. 7 shows the effect of back gate bias on 9Mb test array measurements.

Parasitic slow transient effects

It was found that the number of array fails is sensitive to the delay between applying Vsub and starting array measurements (Fig. 8). These slow transients should be suppressed for T-RAM array to be functional immediately after power-up. Possible root causes of slow transients include RC delays in the substrate and substrate depletion and inversion. An important point is that commercially available SOI wafers typically have very low substrate doping (~1-2x10^{15} cm^{-3}, p-type), which makes them vulnerable to depletion. A low doped substrate may not supply the voltage to the region of substrate beneath the TCCT. The substrate may be even inverted if the voltage difference between the top Si layer and substrate exceeds threshold voltage of BOX MOS capacitor (where Si layer plays the role of gate). Since there is not good electrical contact to the inversion layer, its generation may take a very long time (especially at low temperatures) when voltages are changed.

To verify the mechanism of slow transients, we performed measurements on the test structures comprising large area BOX MOS capacitors. Figure 9 shows measured transient current in response to step-like voltage signal. With positive Vsub (substrate in accumulation), no slow transients were observed. For negative Vsub, very slow transients were measured with time constant on the scale 10-100 s. Time constant was greatly reduced at high temperatures or under illumination. This confirms that the root cause of slow transients is due to slow generation of the electron inversion layer, which is sped up by increased generation in the depletion region by high temperature or light.

Substrate doping for suppressing slow transients

To suppress parasitic slow transients, substrate inversion should be avoided. This can be accomplished by high doping of the substrate near its interface with the BOX. Impurity concentration should be high enough to make BOX MOS threshold voltage much higher than applied voltage. High doping can be achieved either by using SOI wafers with heavily doped substrate, or by ion implantation of impurities into substrate through the top layers (Fig.10). Figure 11 shows the results of TCAD simulations of MOS structure with low (10^{15} cm^{-3}) and high (2x10^{17} cm^{-3}) substrate doping. Vsub=-3V was applied to the substrate at time t=0, and transient current was calculated. At Vsub=-3V, the low doped substrate is inverted and there is a significant voltage drop in the substrate due to depletion. It takes a very long time (>10 s) to establish a steady-state condition. None of these effects are present in a high doped substrate.

T-RAM arrays were fabricated on highly doped substrates (using blanket ion implantation). Implantation conditions were optimized to achieve high doping near the BOX, while avoiding implantation tail in the top Si layer. Array results shown in Fig.12 clearly confirm that the slow transient problem has been eliminated.

References

[1] F.Nemati et al., IEDM Tech. Digest, p.273, 2004.

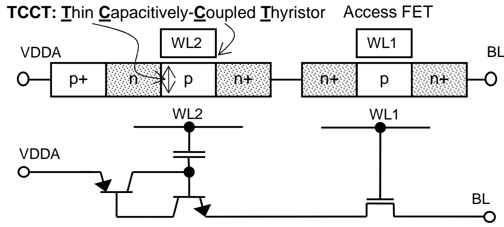


Fig. 1: Structure and equivalent circuit model of T-RAM cell.

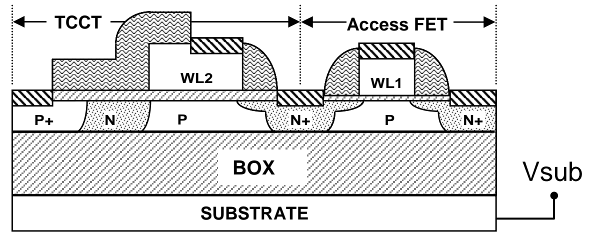


Fig. 2: Cross-sectional diagram of planar SOI T-RAM cell.

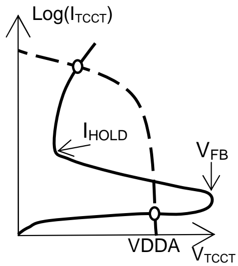


Fig.3. Load-line diagram of T-RAM cell.

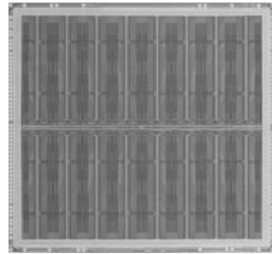


Fig. 4: Image of 9Mbit T-RAM test chip with full SRAM functionality.

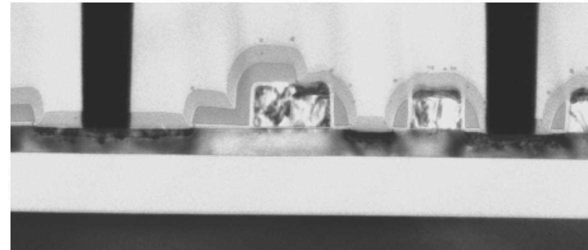


Fig. 5: Cross-sectional TEM image of T-RAM cell implemented in standard 130nm SOI technology.

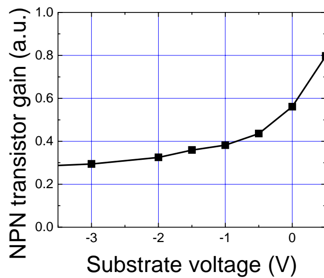


Fig. 6. Vsub dependence of NPN gain.

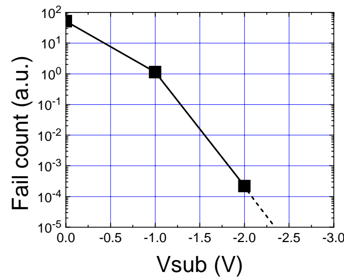


Fig.7. Array fail count vs back-gate bias Vsub.

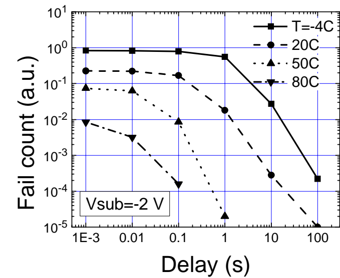
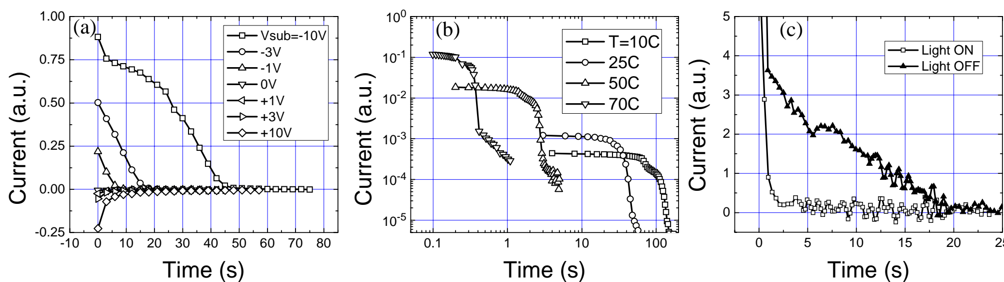


Fig.8. 9 Mbit array fail count vs delay between Vsub and measurements.



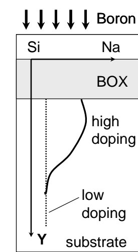
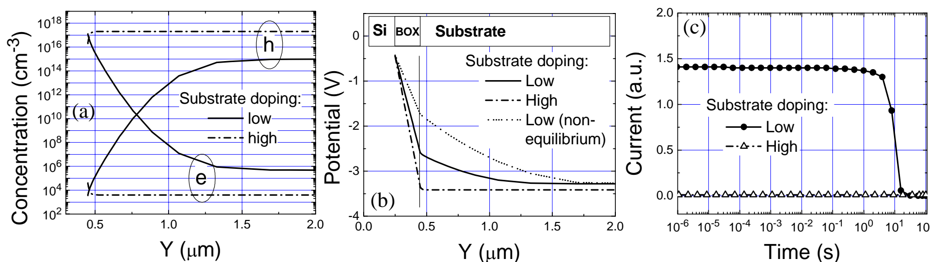


Fig.9. Transient current in MOS capacitor in response to a step-like voltage signal (SOI Si layer – gate, BOX – oxide, substrate – semiconductor) for different conditions: (a) applied voltage, (b) temperature, and (c) illumination.

Fig.10. SOI substrate doping diagram.



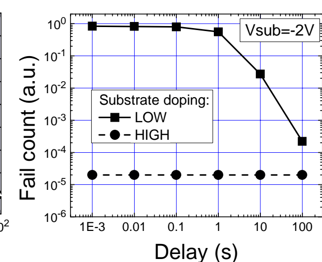


Fig.11. TCAD simulation results at Vsub=-3V: (a) electron and hole concentration, (b) potential (dotted line - right after applying Vsub), and (b) transient current - for low (1e15 cm-3) and high (2e17 cm-3) doping.

Fig. 12. 9 MBit array fail count for low and high doped substrate.