A novel capacitor-less DRAM cell using Thin Capacitively-Coupled Thyristor (TCCT)

Hyun-Jin Cho, Farid Nemati, Rich Roy, Rajesh Gupta, Kevin Yang, Maxim Ershov, Srinivasa Banna, Marc Tarabbia, Craig Salling, Dennis Hayes, Anurag Mittal, Scott Robins
T-RAM Semiconductor, 100 Headquarters Dr., San Jose, CA 95134, P:(408)597-3628, F:(408)597-3601, hjcho@t-ram.com

Abstract

A novel capacitor-less DRAM cell using a thin capacitively-coupled thyristor (TCCT DRAM) is introduced. Experimental results from unit memory cell fabricated in a 130nm SOI logic technology demonstrate Ion/Ioff ratio of 10^7, non-destructive Read, Write speed less than 2ns at 125C, and solid retention characteristics. These cell characteristics combined with a small cell area (as low as $9F^2$) and simple process integration make TCCT DRAM a suitable candidate for high-performance high-density embedded or standalone memory applications.

Introduction

Various implementations of a capacitor-less DRAM cell based on MOSFET floating body effect in SOI or bulk have been previously reported [1,2]. Although this cell concept has a small cell size and a simple integration into CMOS technology, there are major issues to be addressed. The reported cell current margins for narrow-width cells are small (<5uA/cell) and ratio of Ion/Ioff or Iread(D1)/Iread(D0) is less than 10. Such small cell current margins result in a slow read operation and/or manufacturability issues in the presence of large variations that are typical of deep sub-micron MOSFETs. Moreover, the read operation is reported to be quasi-destructive, which can result in further loss of performance. Since the impact ionization or GIDL effect is the major write mechanism for the cell, reported write speed is slow (>10ns). In this paper, we present for the first time a novel capacitor-less DRAM cell that uses a Thin Capacitively Coupled Thyristor (TCCT) instead of a MOSFET. In addition to a small cell size and a simple integration in SOI CMOS flow, TCCT DRAM benefits from a very large Ion/Ioff current ratio ($>10^7$) and a non-destructive read that enable high read speed, as well as a fast write speed (<2ns) enabled by the TCCT device. These unique features provide a simple, logic compatible, high speed, and high density memory.

Thin Capacitively Coupled Thyristor (TCCT)

The concept and characteristics of a TCCT device have been previously reported [3]. A TCCT device consists of a thyristor and gate capacitor connected directly above its p-base region. Fig.1 shows a schematic diagram of the TCCT device and its planar SOI implementation. Fig. 2 shows the typical bi-stable I-V characteristics of a TCCT. The device structure of a TCCT combined with its novel gate-assisted switching addresses the problem of slow switching speed observed in conventional thyristors and enables a TCCT device to be programmed at a very high speed. TCCT programming speed has already been demonstrated using a 9Mb T-RAM test chip that showed a switching speed <2ns for slowest of the 9 million TCCT devices on chip in the temperature range of 0C to 125C [4].

TCCT DRAM Cell Concept

The new TCCT DRAM memory cell is constructed using three control lines; bit line, word line, and write enable line. The schematic 2x2 memory array and layout are shown in Fig. 3 and Fig. 4. The anode node is connected to a bit line (anode line) and the cathode node is connected to a word line (cathode line). The gate poly line itself functions as a write enable line (gate line). A cell size as small as $9F^2$ can be achieved (F is bit line half-pitch). The basic read/write operation is illustrated in Fig. 5. In standby mode, both anode and cathode lines are at Vdd and the stored cell data is maintained by the charge state of the P-base of TCCT. The cathode line functions as the word line in TCCT DRAM and activates the TCCT cells along a gate line. For write 1, gate line is pulsed while cathode line is held at ground level, triggering the TCCT device to latch. The bias scheme for write zero operation is the same as write one except that bit line voltage is kept low (Vwrite0) so that the pulsing of the gate line switches the TCCT into its blocking state. For Read operation, the cathode line is held low and the change in the voltage or the current of the bitline is read into a sense amplifier.

Device Fabrication

TCCT DRAM cells were fabricated in a 130nm SOI CMOS logic technology by only adding three photo/implantation steps to define various regions of the TCCT. Note that there is no addition or change in thermal processes for TCCT device fabrication. Cross sectional TEM image of (a) poly and (b) active regions are shown in Fig. 6.

Transient Measurement

Transient measurements were conducted on single TCCT DRAM cells, using the set up described in Fig. 7. Two different configurations are used for the test, cathode load (Type-1) and anode load (Type-2). Type-1 measurement emulates cell bias conditions during a basic read/write operation while Type-2 measurement emulates cell bias conditions in Standby in order to measure cell data retention characteristics. In both cases, the cell data state is monitored by measuring voltage at the load resistor.

0-7803-9269-8/05/$20.00 (c) 2005 IEEE

Results and Discussion

A. DC characteristics

Fig. 8 is the distribution plot of measured Ion and Ioff currents for a TCCT DRAM cell with W/L = 250nm/180nm at 25C and 125C. Ion/Ioff ratio of more than 10^7 and good TCCT stability at temperatures up to 125C is obtained.

B. Read/Write operation

The Read/Write cell operations were verified at temperatures up to 125C (Fig. 9). Successful write one/zero were detected by monitoring the voltage level at the load resistor. The ON current level was about 120uA/cell consistent with measurement in Fig. 8. Turn on/off speed was measured down to 2 ns and is limited by the test setup bandwidth. As shown in Fig. 10, good Write operation was obtained at the gate pulse width of 2ns. The gate coupling effect on write zero was investigated extensively. Fig. 11 is the V(bitline)/V(gate) shmoo plot conducted at 25C and 125C. More negative bias is required to turn off the TCCT successfully with increasing V(bitline). The V(bitline)/V(gate) margin is reduced as the temperature is increased. This is attributed to increasing TCCT gain at high temperature.

C. Data Retention Characteristics

For data 1, no refresh operation is needed as the stored charge in the P-base of TCCT does not leak out under the standby condition: Vanode = Vcathode = Vdd. However, the P-base charge state for data zero can be gradually lost due to J2 and J3 junction leakage path. Therefore, data zero requires refresh operation. These refresh characteristics were investigated with MEDICI simulation. As shown in Fig. 12, after writing zero, P-base potential is gradually increasing with time. When the P-base potential reaches around 0.6V, TCCT loses the data zero information. The refresh time is strongly dependent on the temperature as leakage currents increase exponentially with temperature.

Data zero refresh times are measured in various temperatures and voltages. Fig. 13 is the measured waveform of the D0 retention test. At the beginning of the test cycle, basic Read/Write operations were conducted and followed by a long holding mode. This measurement is repeated for various holding times to find the maximum holding time at which the data zero retention passes. In Fig. 13, Vout stays high at read operation (Vk = 0V) indicating that a successful D0 retention is achieved with refresh time of 266 ms at 85C.

Fig. 14 shows the data zero retention time at various temperatures at three different anode (bitline) voltages. There is a maximum holding time limit of 1.5sec in the test set-up. All tests below 45C reached this limit. Fig. 14 shows that refresh time decreases exponentially with temperature indicating that the junction leakage is the main source of the D0 retention.

D1 retention characteristics were also monitored in various voltages and temperatures. No data one loss was observed in the temperature range from 0C to 125C. These results confirm that no data one refresh is needed for the TCCT DRAM.

D. Non-destructive Read Characterization

Multiple cycles of read test were conducted in order to investigate any potential Read disturb problems. Fig. 15 shows that no D1 Read disturb was observed even after 4k cycles of repeated Read operation. D0 read disturb test was performed as well and no D0 read disturb problem was found.

E. Write Disturb Characteristics

There are no disturb conditions associated with the pulsing of gate line because gate pulsing only occurs during a write event. Cell cannot be disturbed by the cathode line pulse as well, as the cathode nodes of adjacent cells are electrically isolated from each other. There is however a disturb condition associated with the pulsing of the bit line. When one cell is continuously under write zero, the other cells in the same bit line undergo voltage drop, which can result in the P-base charge to leak out through the J1 junction. Such bit line disturb condition can be minimized by avoiding a Vwrite0 level that results in excessive voltage drop in the anode line. Fig. 16 shows the measured write characteristics at various Vwrite0/Vg levels. It is observed that for Vdda/Vg=1.2V/-1.5V condition, successful turn off is achieved at Vwrite0 = 0.8V, which can minimize the bit line disturb effect.

Conclusion

The basic cell specification is summarized in Table 1. These unique features demonstrate that TCCT DRAM cell is a promising memory technology for future high-density high-speed memory applications.

Table 1: TCCT DRAM cell characteristics

Ideal Cell Size	$9F^2$
Process	SOI Logic process
Data 1 Cell current	120 uA/cell
Datat 0 Cell current	0.1 pA/cell
Cell Leakage at Standby	0 A/cell
t_write_zero	2 ns
t_write_one	< 0.5 ns
Max. positive voltage	+1.2V
Max. negative voltage	-1.5V
Data zero refresh time	266 ms @85C
Data one refresh	Not required

References

(1) T. Ohsawa et al., 2005 ISSCC, pp. 458.
(2) R. Ranica et al., 2005 VLSI Tech. Dig., pp. 38.
(3) F. Nemati et al., 1999 IEDM Tech. Dig., pp. 283.
(4) F. Nemati et al., 2004 IEDM Tech. Dig., pp. 273.

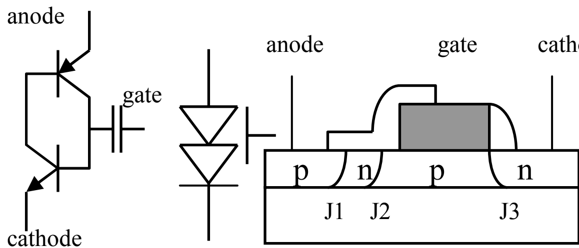


Fig. 1: Equivalent circuit model of TCCT memory cell and schematic structure of memory cell built on conventional SOI technology. Additional implantation processes are needed to form two junctions, J1/J2 over CMOS process.

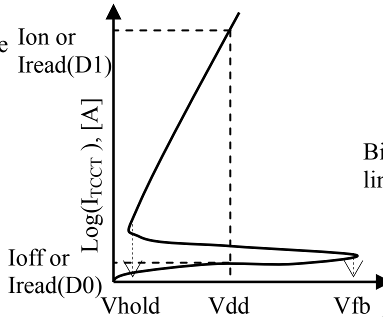


Fig. 2: Typical IV curve of thyristor device showing bi-stable behavior.

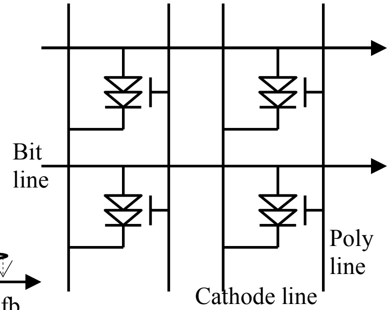


Fig. 3: Schematic diagram of 2x2 memory array. Anode is connected to the bit line (anode line). Cathode is connected to the word line (cathode line). Gate is connected to the write enable line (gate line).

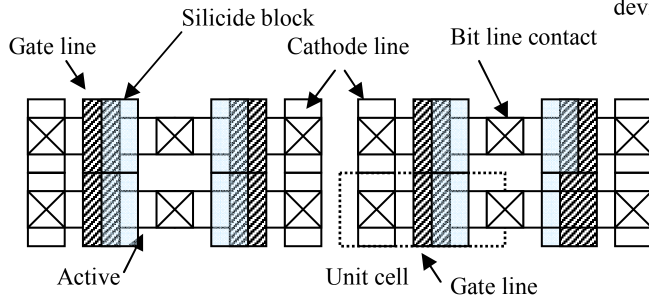


Fig. 4: TCCT DRAM cell layout. Cathode line (word line) and Gate line (write enable line) are in the same direction. Bit line is in the perpendicular to the Gate line. The unit size is $9F^2$, where F is a half pitch of the bit line. Silicide block layer is used to form p/n junction in the anode side.

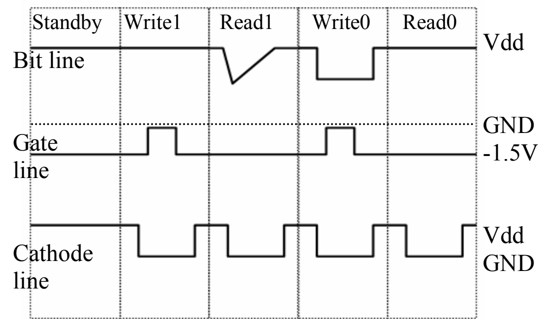


Fig. 5: Memory cell operation diagram. At standby, both bit line and cathode lines are Vdd and gate line is at negative voltage. Cells are activated by grounding the cathode line (Word line). Gate line is pulsed during both write zero/one events. The bit line level is used to Read the high impedance (read zero) or low impedance (read one) states of the cell.

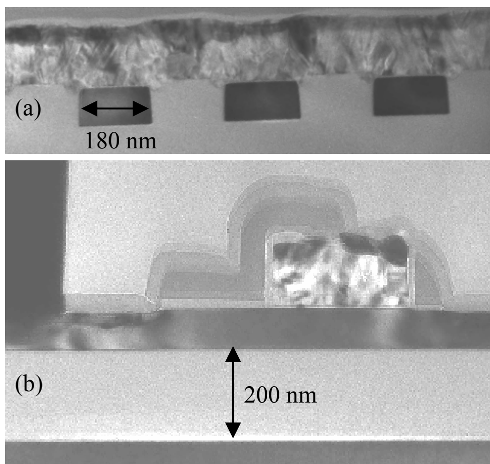


Fig. 6: XTEM image of TCCT device fabricated with 130nm SOI logic process; (a) active, (b) poly. The gate length in the study is 250nm. The width of the active is 180nm. SOI and BOX thickness is 100nm and 200nm, respectively. Conventional silicidation process is used in the array cell.

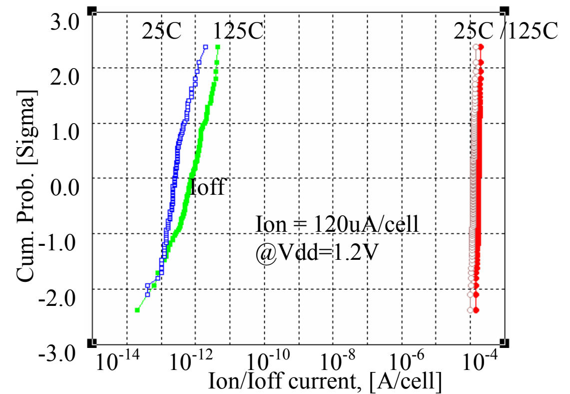


Fig. 8: Ion/Ioff characteristics measured from single TCCT device. W/L of device is 180/250 nm. The ratio between Ion/Ioff is more than 10^7 at 125C. Thermally stable TCCT is achieved at 125C.

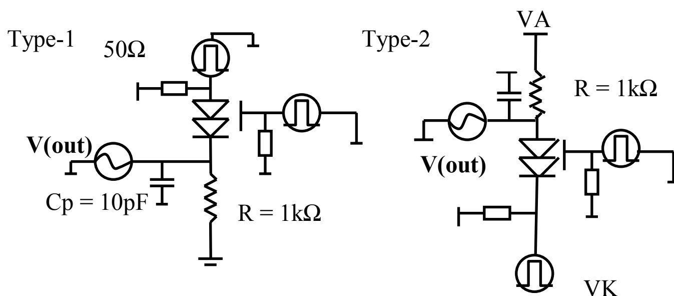


Fig. 7: Two set-up scheming for the transient measurement; load resistor in the cathode node (Type-1) and anode node (Type-2). Type-1 is used for basic cell read/write operation while Type-2 is used for retention characteristics. Current of the device is monitored by measuring voltage at load resistor. Output RC delay is in the order of few ns, which limits the measurement of actual turn on/off time.

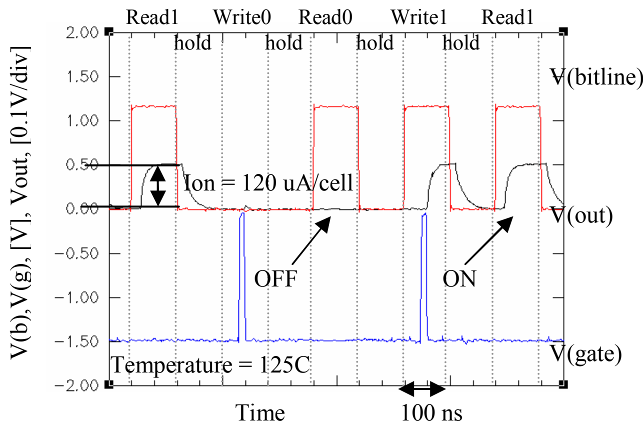


Fig. 9: Memory cell operation measured from single TCCT device at 125C. At ON state, current pass thru the load resistor and detected by the oscilloscope. The measured ON current is ~120 uA/cell. V(gate) is pulsed from –1.5V to GND during Write, triggering TCCT turn-on/turn-off.

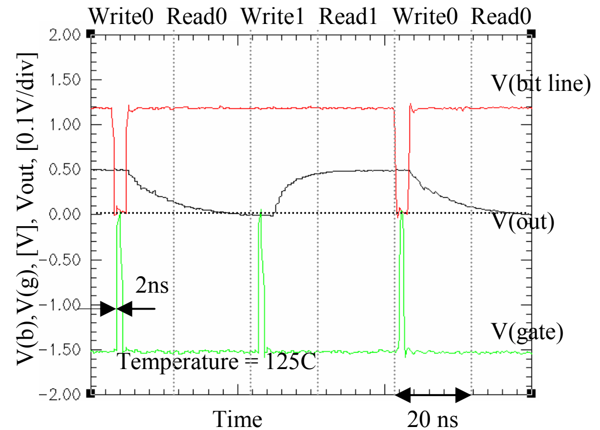
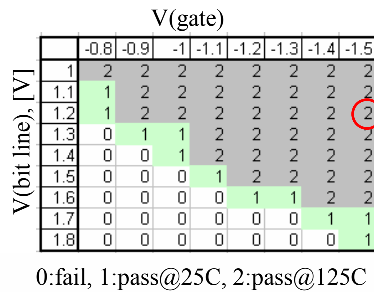


Fig. 10: Measured wave form of TCCT switching ON/OFF. Gate-assisted switching off is achieved with pulses as narrow as 2ns. The delay in the V(out) to reach its final value is a result of the parasitic RC delay of the measurement setup.

Fig. 11: Read/Write shmoo plot of the V(bit line) and V(gate) at 25C and 125C. Increasing V(bit line) requires more gate coupling. Margin for hot temp. is reduced due to high TCCT gain. The optimum condition is V(bit line)/V(gate) = 1.2V/-1.5V



V(gate)

V(bit line), [V]	-0.8	-0.9	-1	-1.1	-1.2	-1.3	-1.4	-1.5
1	2	2	2	2	2	2	2	2
1.1	1	2	2	2	2	2	2	2
1.2	1	2	2	2	2	2	2	2
1.3	0	1	1	2	2	2	2	2
1.4	0	0	1	2	2	2	2	2
1.5	0	0	0	1	2	2	2	2
1.6	0	0	0	0	1	1	2	2
1.7	0	0	0	0	0	0	1	1
1.8	0	0	0	0	0	0	0	1

0:fail, 1:pass@25C, 2:pass@125C

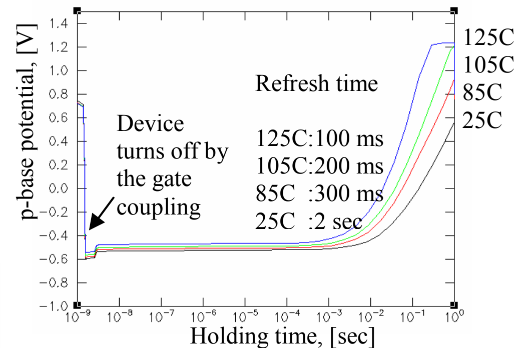
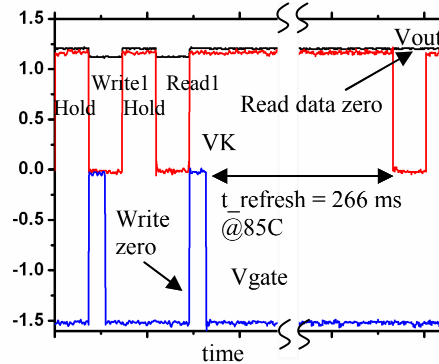


Fig. 12: Data zero refresh characteristics by MEDICI simulation. P-base voltage drop at write zero and gradually increased by the reverse junction leakage current.

Fig. 13: Measured wave form of D0 retention characteristics. W1/Hold/R1 operation was conducted prior to write zero ensuring that cell is properly operating. After the long holding time, Vout level is monitored at VK = 0. In the figure, successful data zero retention is achieved after 266 ms refresh time at 85C.



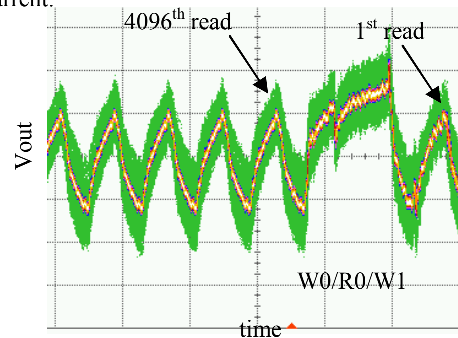


Fig. 15: No degradation of Vout signal is detected after 4096 read/hold cycles compared to 1st Read cycle indicating non-destructive Read.

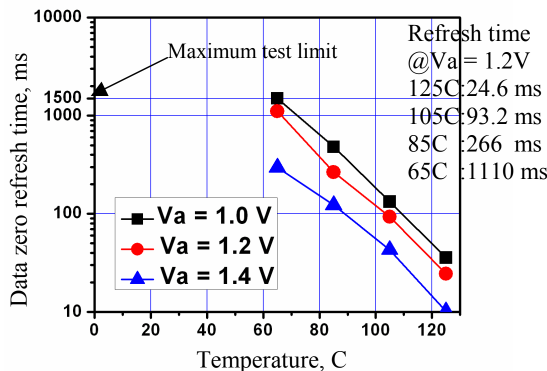
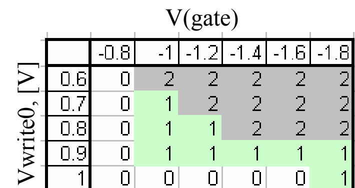


Fig. 14: Data zero refresh time in various temperatures at three different Va condition. The maximum test limit is 1.5 s.

Fig. 16: Read/Write shmoo plot of the V(write0) and V(gate). In order to minimize the bit line disturb, higher V(write0) is preferred. Operation window is narrowed at hot temperature.



V(gate)

Vwrite0, [V]	-0.8	-1	-1.2	-1.4	-1.6	-1.8
0.6	0	2	2	2	2	2
0.7	0	1	2	2	2	2
0.8	0	1	1	2	2	2
0.9	0	1	1	1	1	1
1	0	0	0	0	0	1

0:fail, 1:pass@25C, 2:pass@125C
V(bit line) = 1.2V, V(gate) pulse width = 2 ns.