

Thyristor RAM (T-RAM): A High-Speed High-Density Embedded Memory Technology for Nano-scale CMOS

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Farid Nemati
T-RAM Semiconductor Inc.
Milpitas, CA





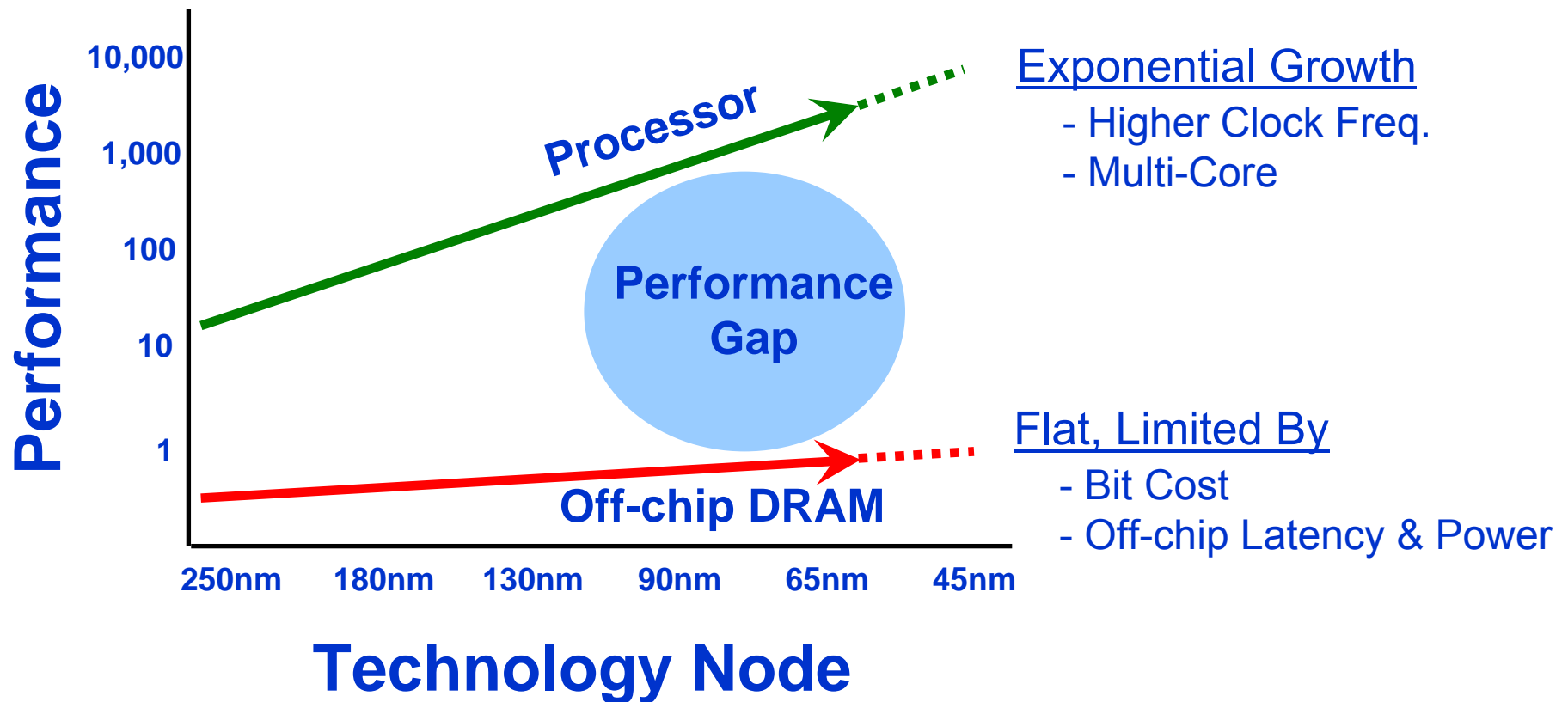
Outline

- ❖ **Embedded RAM Trends & Challenges**
- ❖ **Thyristor-RAM Introduction**
- ❖ **Thyristor-RAM in Embedded Applications**
- ❖ **Thyristor-RAM Current Status**
- ❖ **Thyristor-RAM Scalability & Outlook**



Widening Memory Performance Gap

- Memory Performance Penalty Growing w/ Scaling

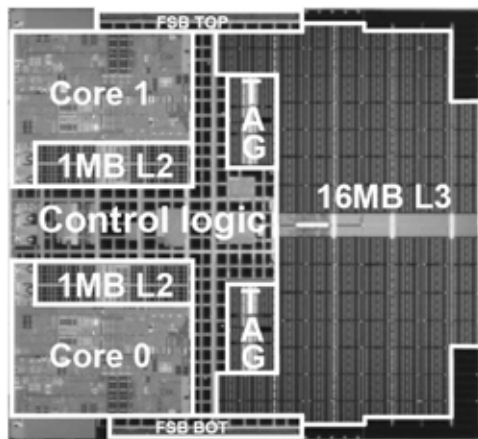


Ref: Based on D. Patterson et al, Hot Chips 1996



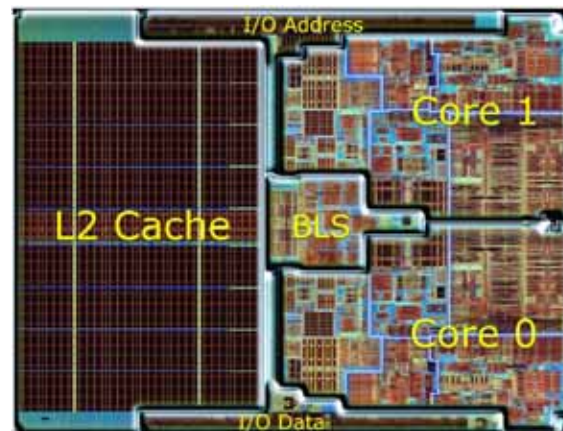
Memory Sub-system Trends

- Widening Off-chip RAM Gap → Larger, More Caches On-chip
- Die Fraction Taken-up by Embedded RAM Approaching 50%
 - Impacting All Data Processing App's: MPU, DSP, GPU,...
- 6T-SRAM the Single Most Dominant Embedded RAM



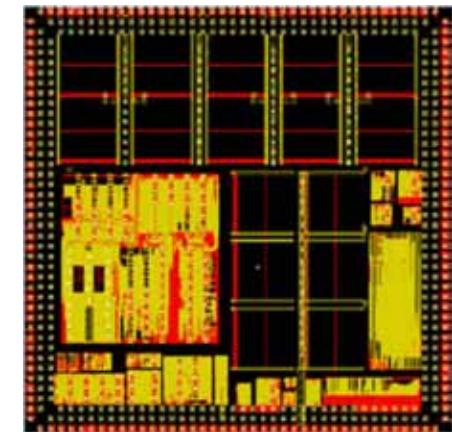
Intel MPU - Xeon

Servers & Workstations
18MB L2+L3, **50%** of Die
65nm, 6T-SRAM
S. Rusu et al, ISSCC 2006



Intel MPU - Core2Duo (Merom)

Desktops & Notebooks
4MB L2, **40%** of Die
65nm, 6T-SRAM
N. Sacran et al, ISSCC 2007



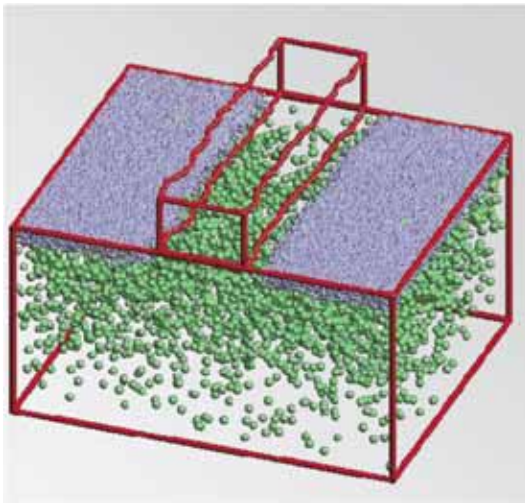
TI DSP - TMS320C6414

Wireless Infrastructure
1MB L2, **40%** of Die
130nm, 6T-SRAM
G. Frantz, UT Seminar 2003

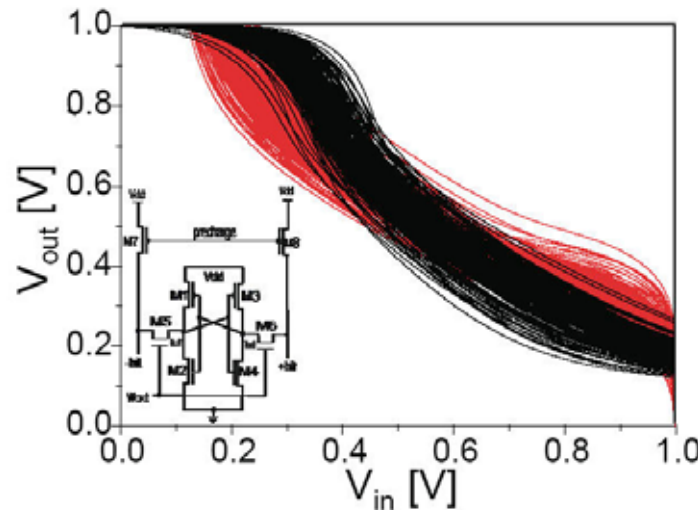


6T-SRAM Stability & Scalability

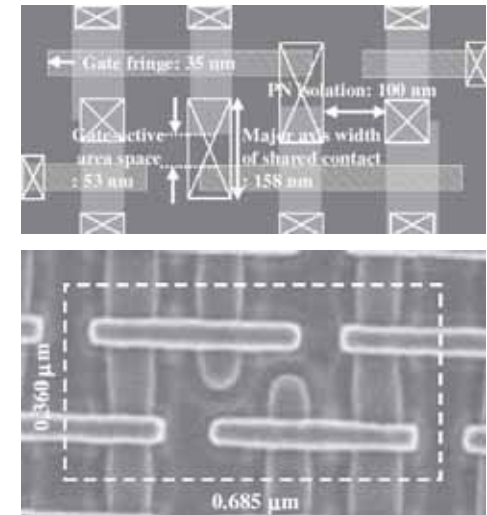
- 6T-SRAM Scaling Severely Limited at 45nm and Beyond
 - Diminished Stability due to Increasing Random MOSFET Variability
 - Complex 6T-SRAM Layout Pattern Pushing Lithography Limits
- Solutions Add Area/Cost/Complexity, e.g., 8T, Assist Features



RDF (Random Dopant Fluctuation) and LER (Line Edge Roughness) Worsen MOSFET Variability w/ Scaling
M. Miyamura et al, VLSI Tech. 2007



6T-SRAM Instability Due to Increased MOSFET Variability w/ RDF & LER in 35nm MOSFETs
A. Asenov, VLSI Tech. 2007



Layout Pattern of a 45nm High Density 6T-SRAM Cell
R. Morimoto et al, VLSI Tech. 2007

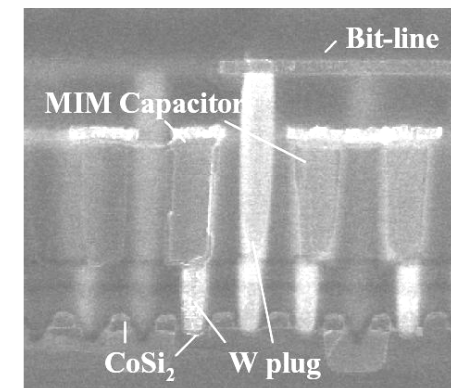
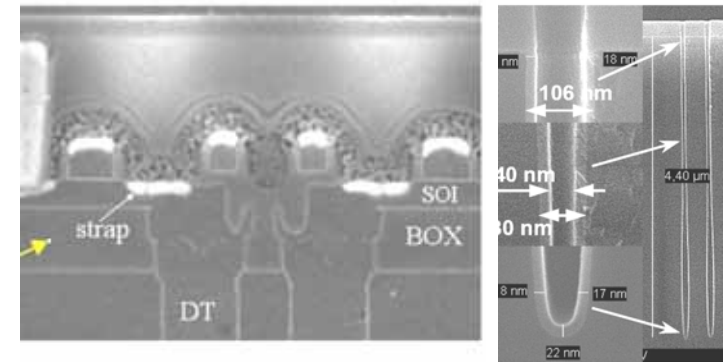
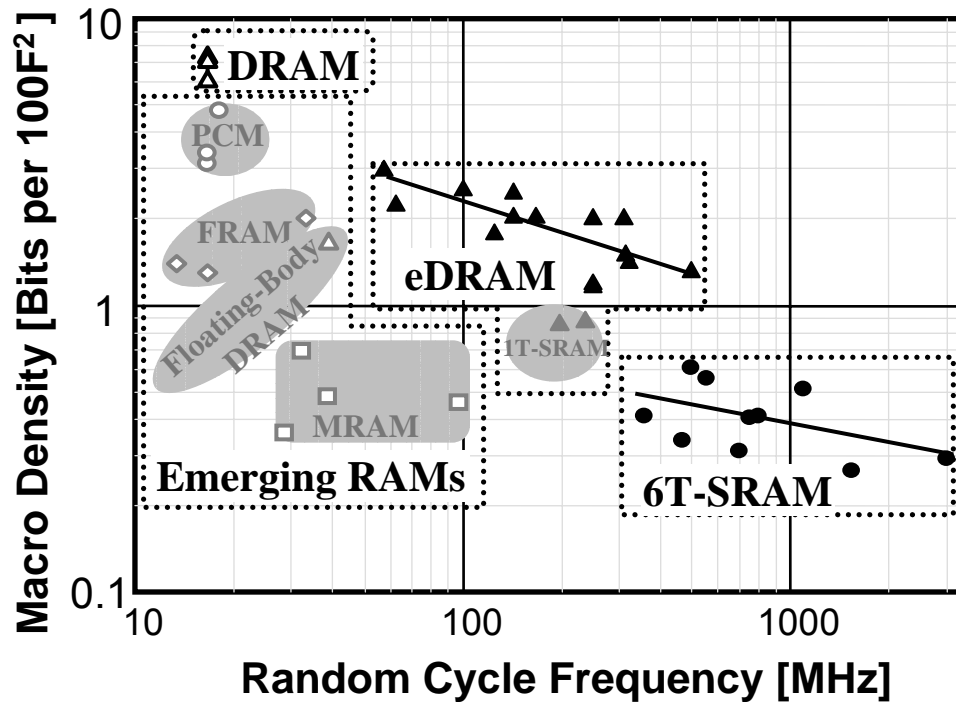


Other Embedded RAM Technologies

Alternative RAM Technologies Unable to Displace 6T

- ❑ Poor Performance: Most are as Slow as Off-chip DRAM
- ❑ High Process Cost and Complexity
- ❑ Scalability and Viability Barriers

Trench or Stacked eDRAM Add Significant Process Cost and Complexity



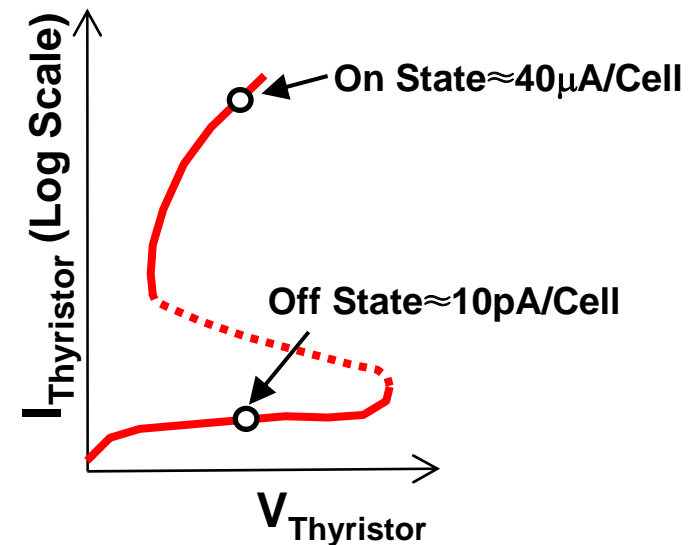
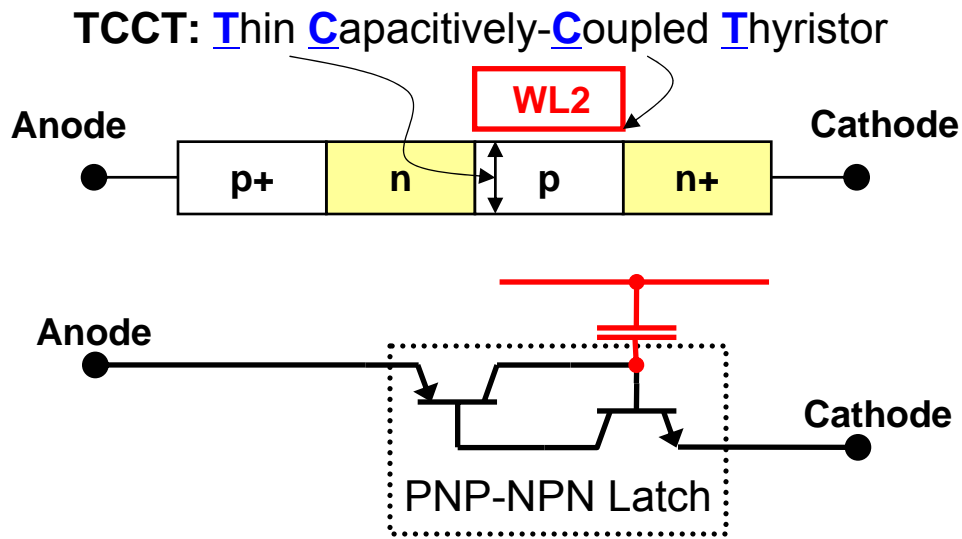
Wang et al, IEDM 2006

Takeuchi et al, VLSI2001



Thyristor Advantages

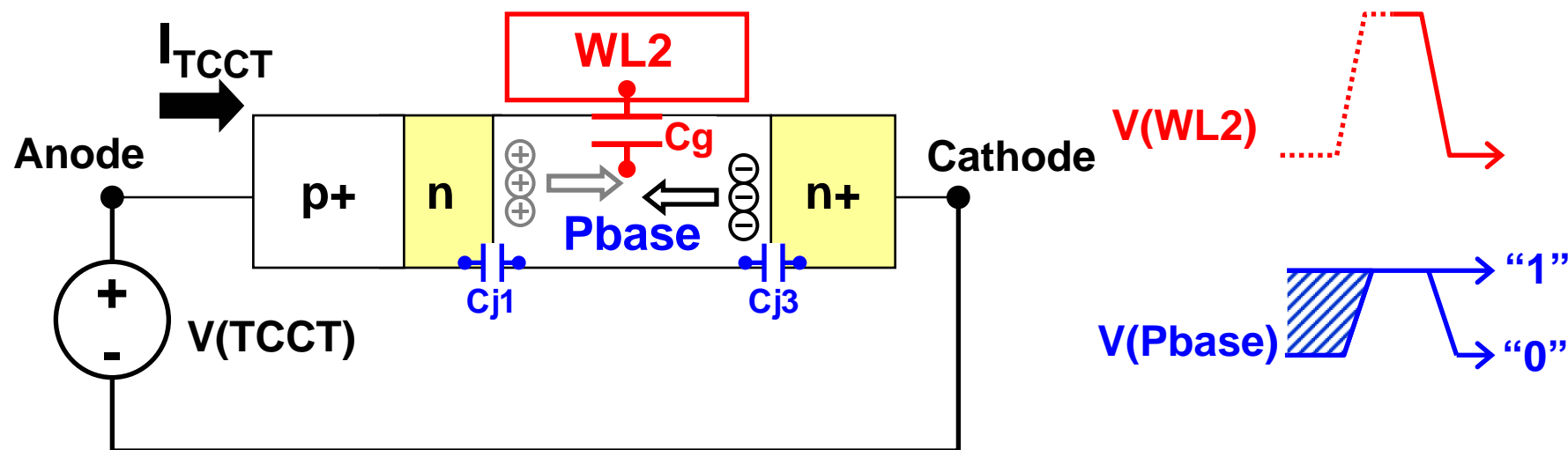
- Internal Latch, Like 6T-SRAM, but 4X Better Density
 - “1T” PNP-NPN Latch Instead of “4T” Latch in 6T-SRAM
- Excellent Read Performance and Margin
 - High Read Current, Non-destructive Read, Read Current Ratio $> 10^6$
- Thin Capacitively Coupled Thyristor (TCCT) \rightarrow Fast Write
 - Over 1000X Faster than Conventional Thyristor





TCCT Fast Write Concept

- ✿ WL2 Rising Edge Capacitively Raises Pbase Potential
- ✿ WL2 Falling Edge Capacitively Programs Pbase
 - ✿ $V_{TCCT} \geq 1V \rightarrow I_{TCCT} \text{ High} \rightarrow C_g \ll (C_{j3} + C_{j1}) \rightarrow \text{Pbase Hi}$
 - ✿ $V_{TCCT} \leq 0.5V \rightarrow I_{TCCT} \text{ Low} \rightarrow C_g \gg (C_{j3} + C_{j1}) \rightarrow \text{Pbase Lo}$

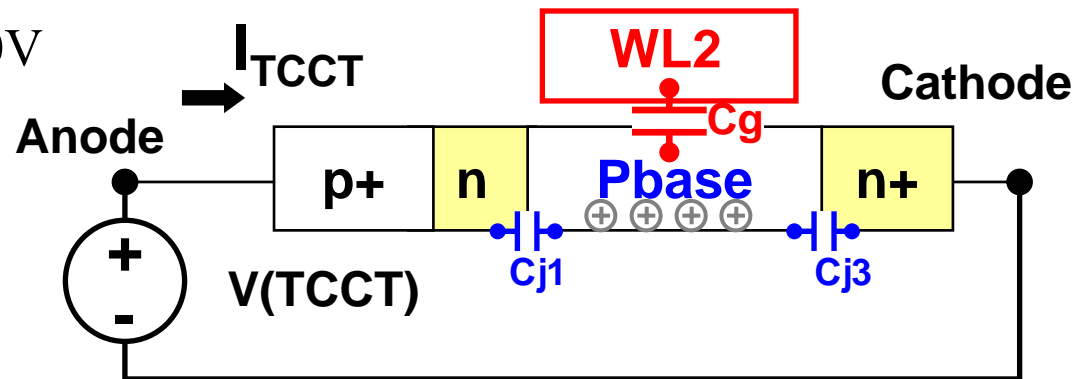




Thyristor-RAM Read & Retention

Standby:

- Thyristor Off, $V_{TCCT} \approx 0V$
- “1”: $V(\text{Pbase})$ High
- “0”: $V(\text{Pbase})$ Low
- $I_{TCCT} \approx \text{pA}$

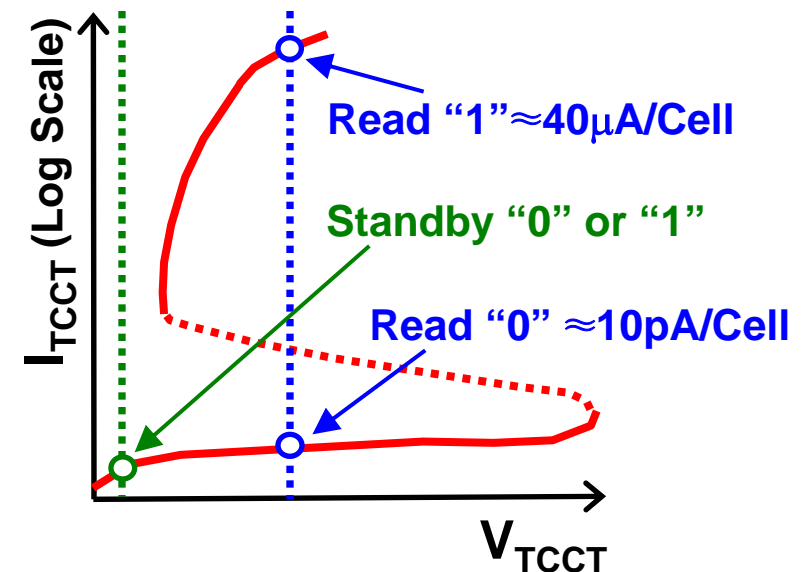


Read Operation:

- Activate Thyristor, $V_{TCCT} \geq 1V$
- Thyristor Latches if Pbase High
- Thyristor Blocking if Pbase Low

Data Retention:

- Periodic Restore or Refresh

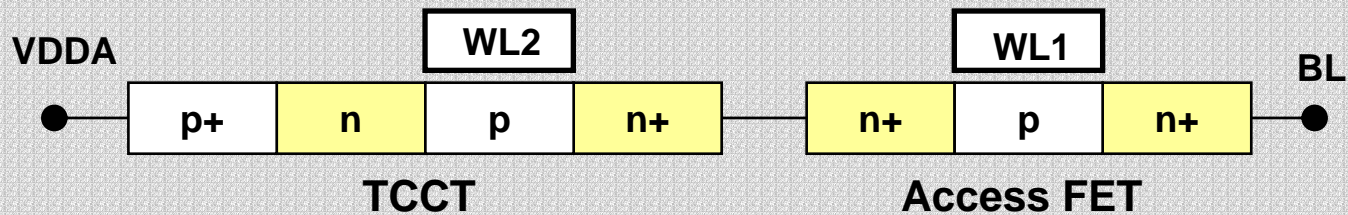




Thyristor-RAM Cell Variants

1: Thyristor-SRAM (T-SRAM):

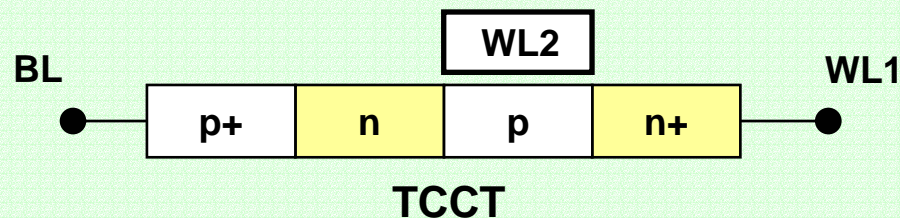
- Two Elements per Cell: 1 TCCT + 1 Access FET
- Hidden Dynamic Restore → SRAM Functionality



Ref: Nemati et al, IEDM 1999, IEDM 2004

2: Thyristor-DRAM (T-DRAM):

- One Element per Cell: TCCT-Only
- Dynamic Refresh → DRAM Functionality

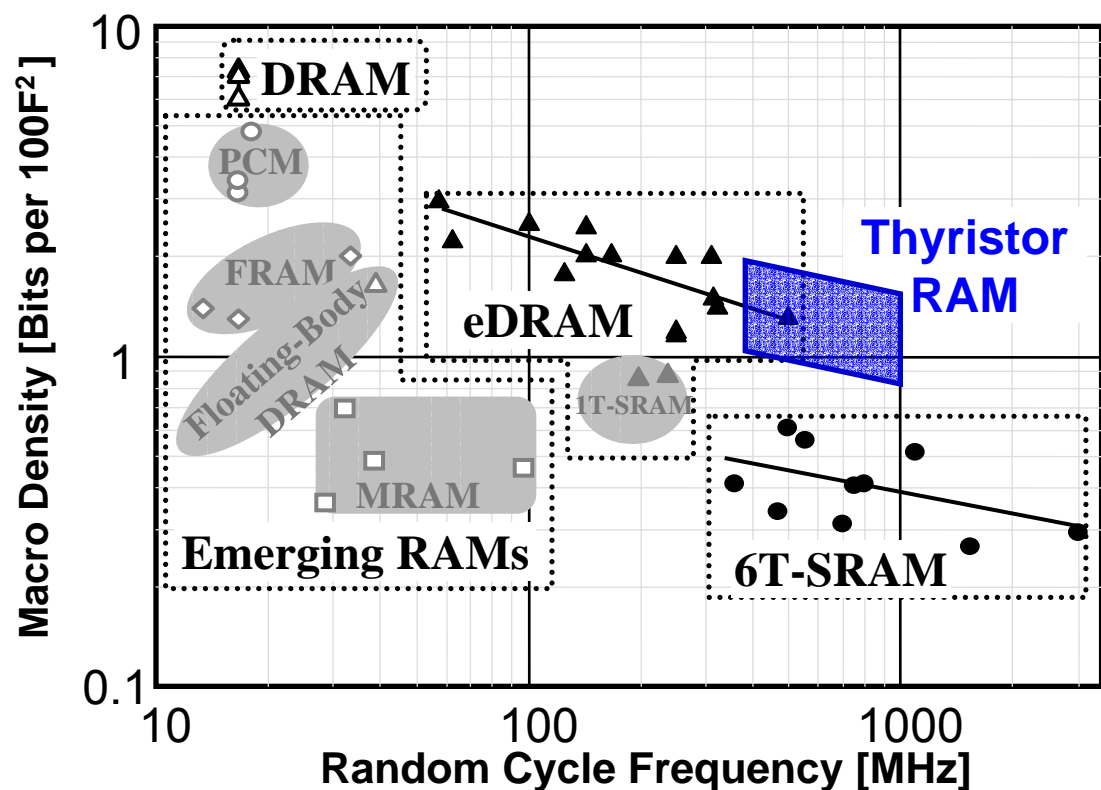


Ref: H.J. Cho et al, IEDM 2005



Embedded Thyristor-RAM Attributes

- ✪ Equals 6T-SRAM Speed at 2.5X Higher Macro Density
- ✪ Active and Standby Power Less or Equal to 6T-SRAM
 - ✪ Standby Power: T-SRAM $\sim 1\text{nA/Cell}$, T-DRAM $\sim 0.2\text{nA/Cell}$

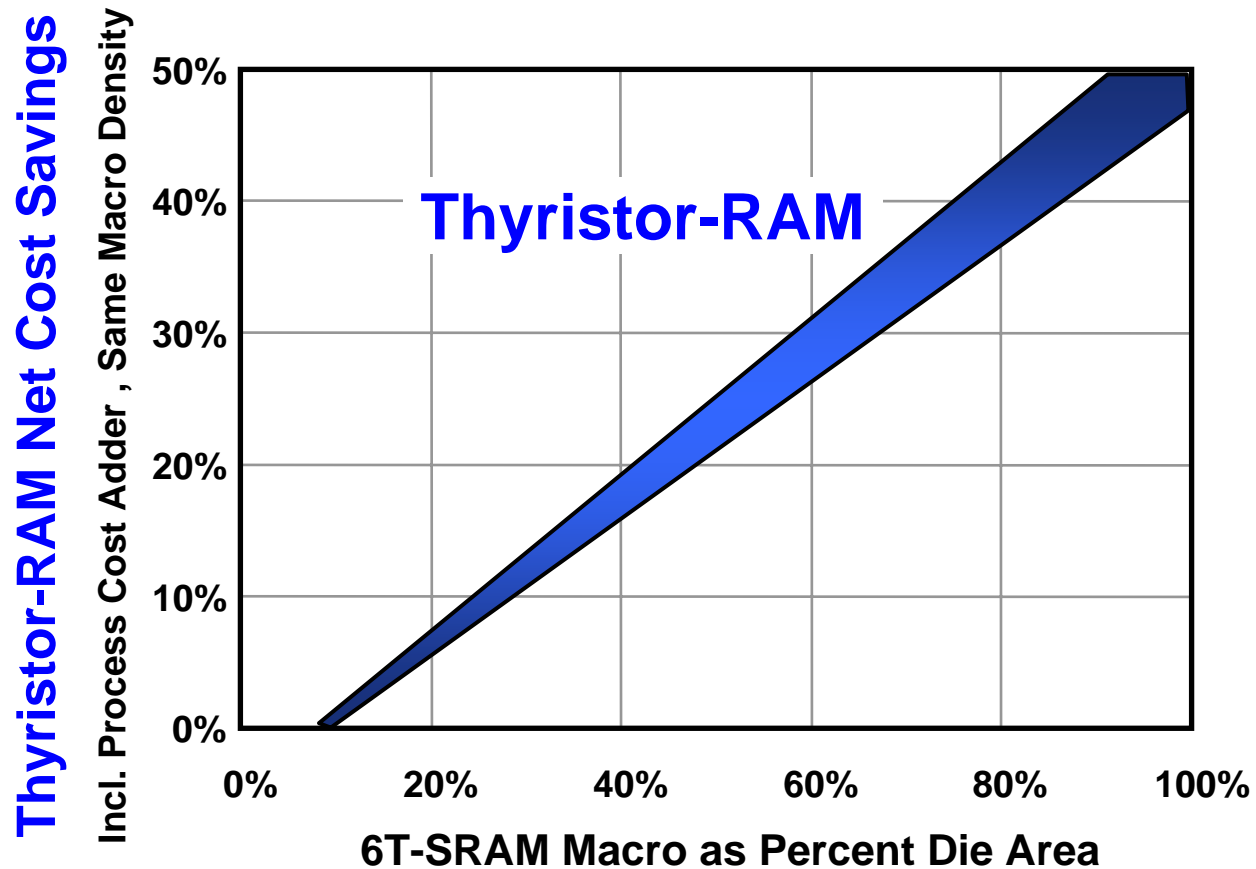


Data Points from 2000-2007 IEEE Conference/Journal Chip/Macro Publications



Embedded Thyristor-RAM Cost Benefit

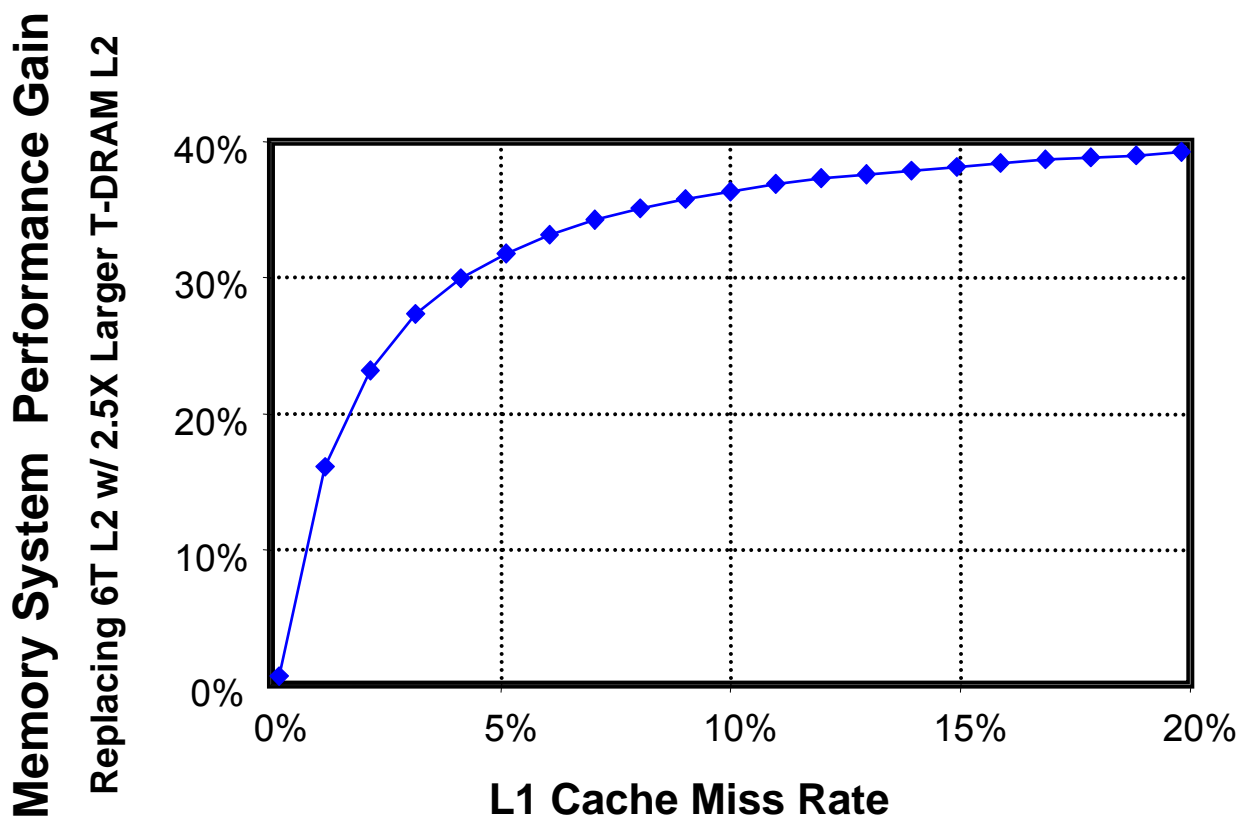
- ✪ Replacing On-chip 6T w/ Thyristor-RAM to Reduce Die Cost
- ✪ No Performance or Power Penalty Compared to 6T





Embedded Thyristor-RAM Density Benefit

- Replacing On-chip 6T w/ Thyristor-RAM to Increase Macro Size
- 2.5X Larger Cache in Same Area → System Performance Gain



Assumptions: L1 Access=0.5, L2 Access=1, Off-chip Access=100, L2 Local Miss Rate ~40%

Miss rate dropping 1.3X per each 2X L2 increase



Thyristor-RAM Technology Status

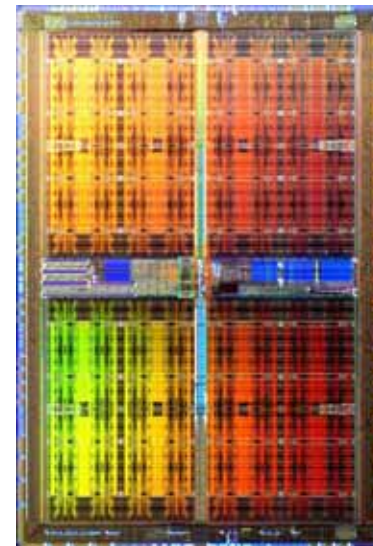
- ✦ Freescale 130nm SOI Logic CMOS as Initial R&D Platform
- ✦ A Toolkit of Technologies Developed to Address Barriers
 - ✦ Knowledge of Nano-scale Thyristor Physics
 - ✦ Process & Device Innovations for High-margin Thyristor RAM Cells
 - ✦ Circuit & Architecture Innovations to Build Thyristor-RAM Macro/Chip
- ✦ Manufacturability Proven in Silicon; Entering Production
 - ✦ Good Stable Yield and Reliability, 2500+ Wafers, 240+ Man-years

Thyristor-SRAM Discrete Product Die

- 18Mb Industry-standard Sync. SDR SRAM
- 130nm SOI CMOS Technology
- 2X smaller die than 130nm 18Mb 6T-SRAM
- Customer Samples 4Q07

References:

F. Nemati et al, IEDM 2004
M. Ershov et al, SOI Conf. 2005
H.J. Cho et al, IEDM 2005
K.J. Yang et al, SOI Conf. 2006
R. Roy et al, ISSCC2006

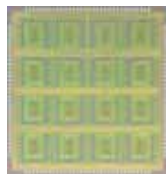




Building the Toolkit – Circuit & Architecture

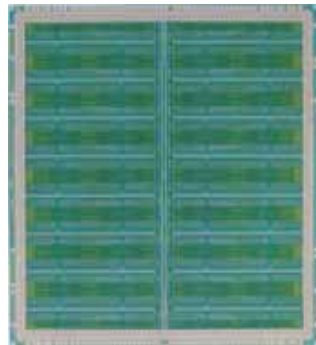
- Series of Chips w/ Added Innovations in Design
 - Bitline Coupling → Bitline Shielding Architecture
 - Periodic Restore → Hidden Restore Architecture
 - Single-ended Cell → High Speed Reference & Sense Amp Design
 - Non-selective WL2 → Fast Write Arch. for Discrete Products

Thyristor-SRAM Test-Chips and Product Chip



1.5Mb

Bitcell Test Vehicle
External Bit Timings
External Bit Voltages



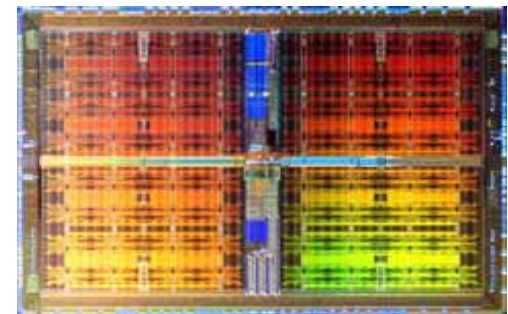
9Mb Array

Bitline Shielding Arch.
Product-like Cell Array
Hidden Restore Arch.



9Mb SRAM

Standard SDR SRAM
Regulators
Redundancy



18Mb SRAM Product

High Speed Ref. & Sense
Fast Write Arch.
2nd Gen. Hidden Restore Arch.

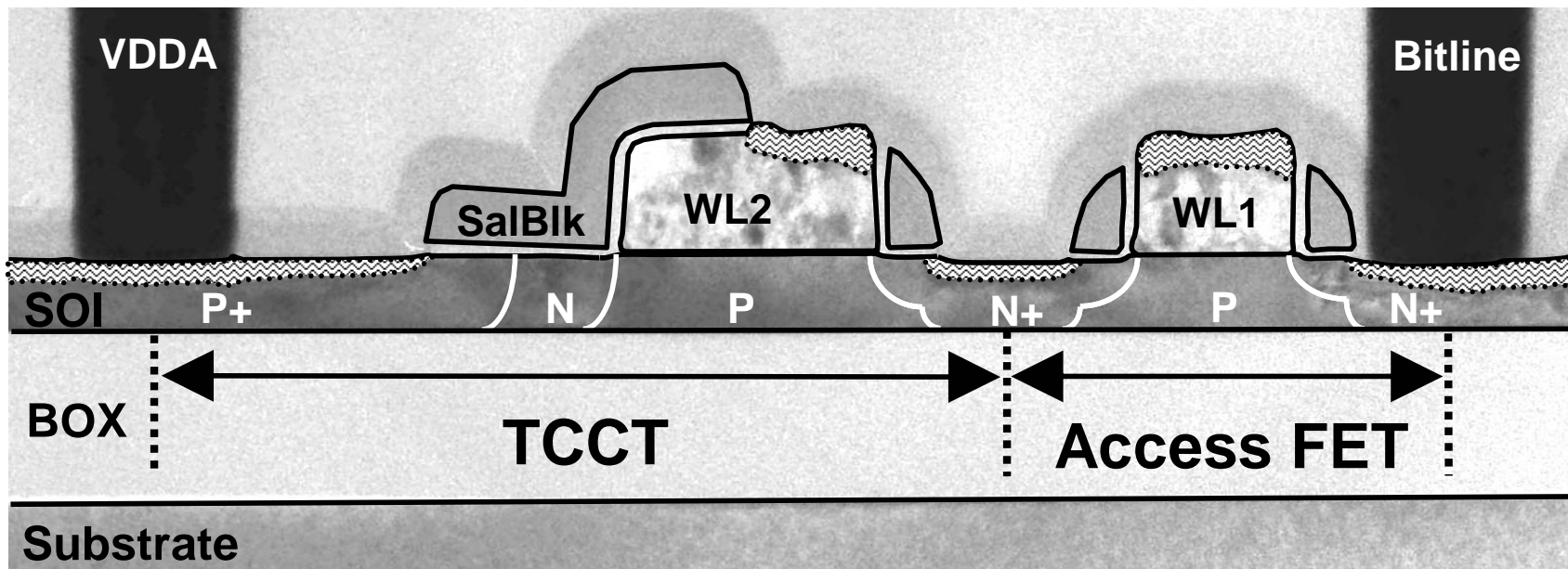
Ref: R. Roy et al, ISSCC2006



Thyristor-RAM Cell in SOI

- ✦ Using Freescale 130nm SOI CMOS Logic Technology
- ✦ Only Extra Implants Required – No DRAM Processing Needed
 - ▣ Added Manufacturing Cost: T-SRAM $\leq 12\%$; T-DRAM $< 5\%$

Thyristor-SRAM Cell Cross-section





Thyristor-RAM vs. 6T-SRAM Cell Area

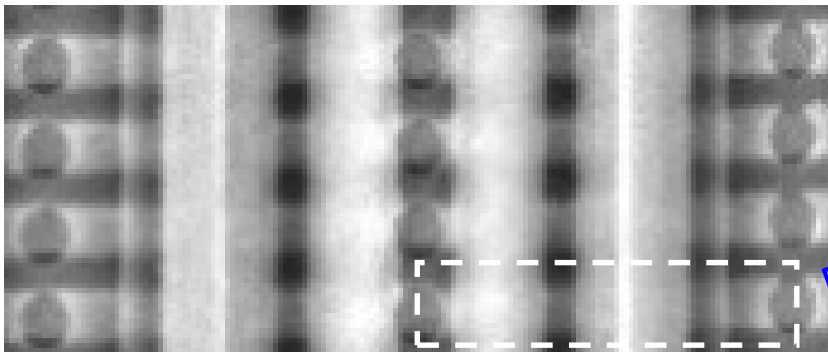
- 4X-5X Smaller Cell at Same Technology Node
- Two Generation Cell Area Advantage over 6T

130nm T-SRAM Area = $0.56 \mu\text{m}^2$

130nm T-DRAM Area = $0.44 \mu\text{m}^2$

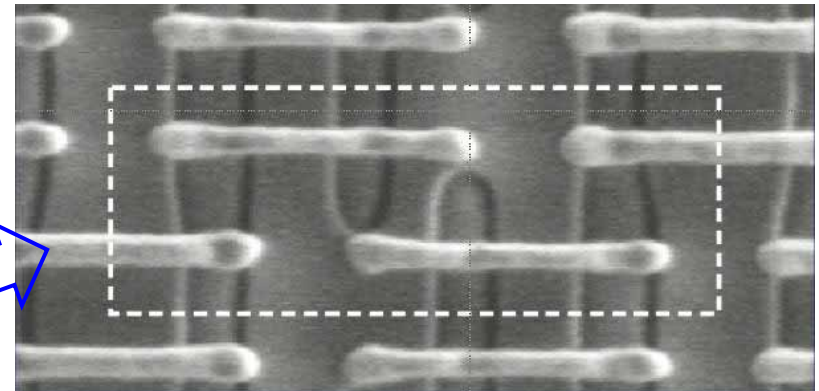
130nm 6T Cell Area = $2.30 \mu\text{m}^2$

65nm 6T Cell Area = $0.56 \mu\text{m}^2$



130nm Thyristor-SRAM Array

4X

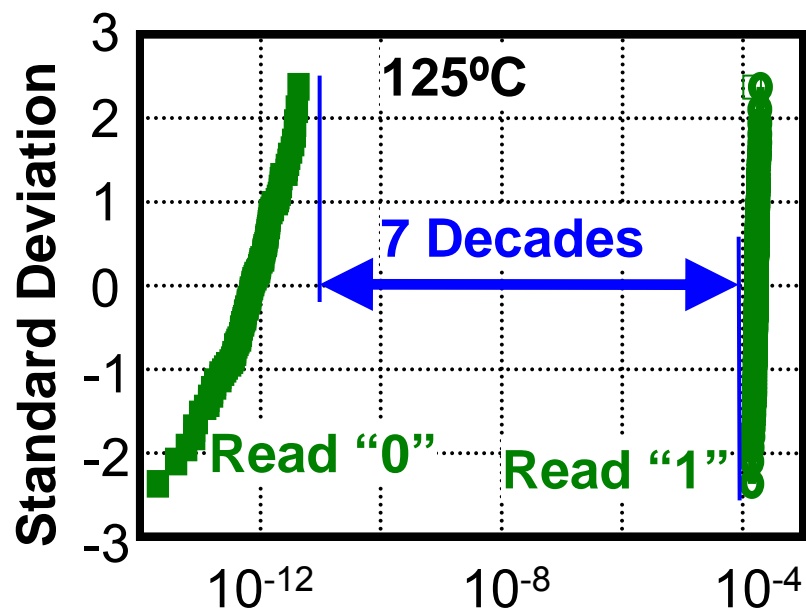


130nm 6T-SRAM Array



Thyristor-RAM Silicon Read Current

- Excellent Read Margins
- High Read Current

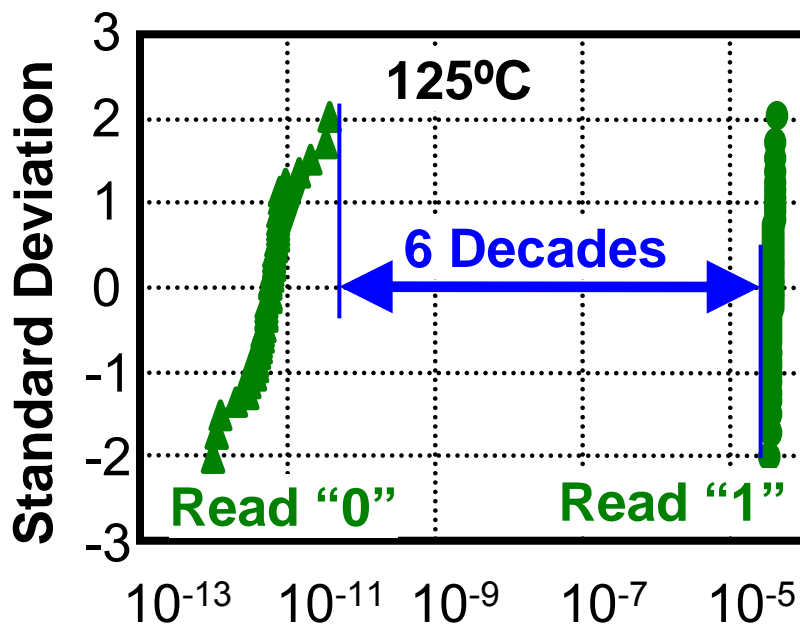


Thyristor-DRAM

Cell Read Current Distr. [A/cell]

Read "1" = $120\mu\text{A}/\text{Cell}$

Read "0" $\leq 10\text{pA}/\text{Cell}$



Thyristor-SRAM

Cell Read Current Distr. [A/cell]

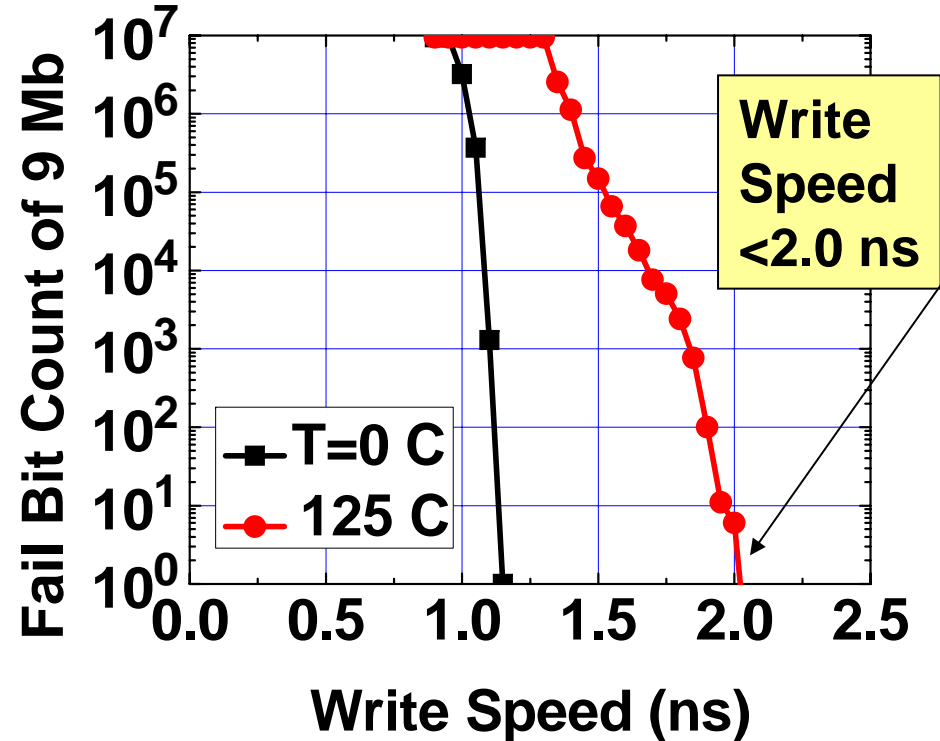
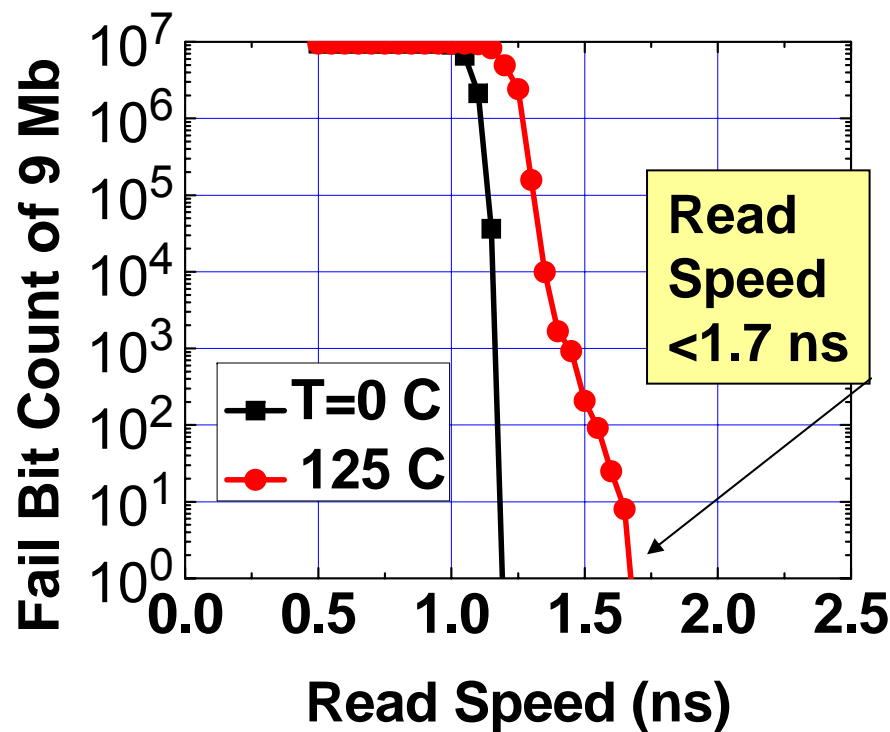
Read "1" = $40\mu\text{A}/\text{Cell}$

Read "0" $\leq 10\text{pA}/\text{Cell}$



Thyristor-SRAM Silicon Performance

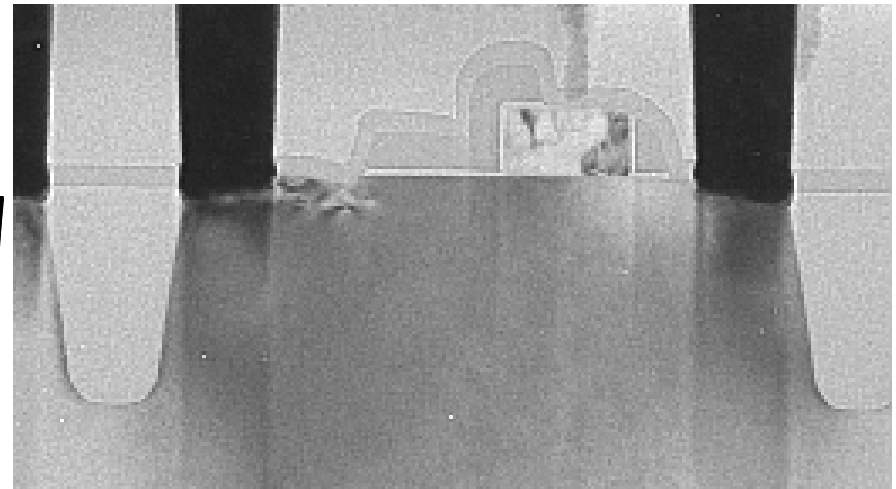
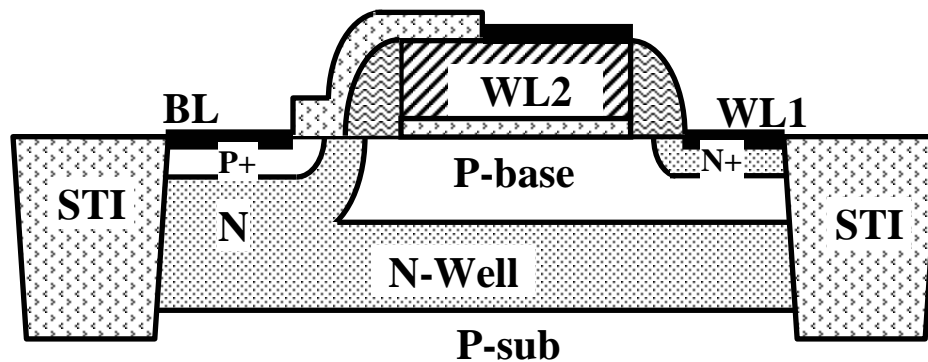
- Cell Array Speed Consistent w/ 500MHz+ at 130nm
 - Random Access, Across Temperature, 5-Sigma Slowest Cells





Next Generation Thyristor-RAM

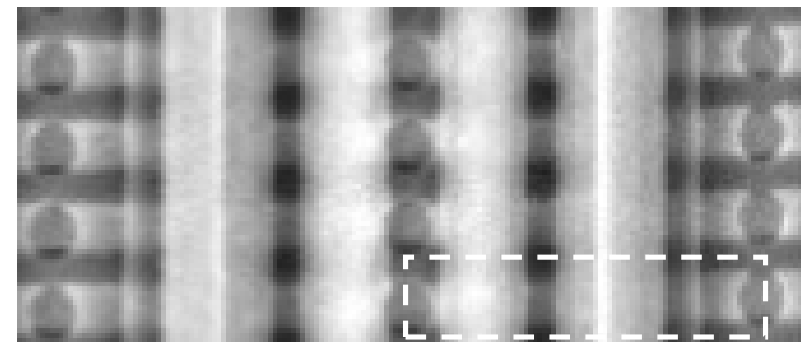
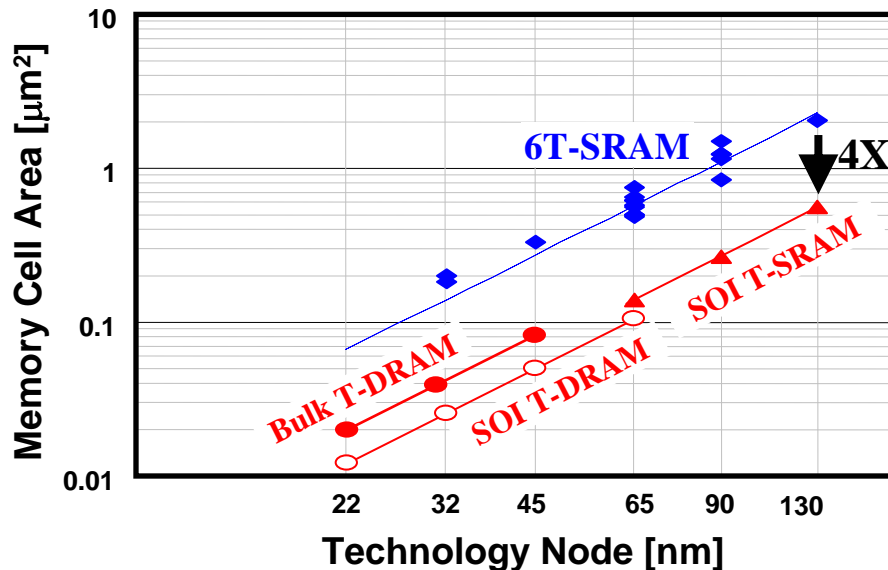
- Planar Bulk Thyristor-DRAM Targeting 45nm & Beyond
- Std Bulk CMOS plus 3 Non-critical Implant Masks
- Concept Proven in Silicon at 130nm
- 45nm Development Started





Thyristor-RAM Scalability

- TCCT Insensitive to FET Variability Limiting 6T-SRAM Scaling
 - Accumulation Mode Device → Minimizes Dopant Fluctuation Effect
 - WL2 Just a Capacitor → Small Sensitivity to Line Edge Roughness
- Planar Thyristor-RAM Cell Area Fully Scalable to 22nm
 - Excellent Read Margin/Stability Maintained at Scaled Dimensions
 - Simple Cell Array Layout Pattern Relaxes Lithography Challenges



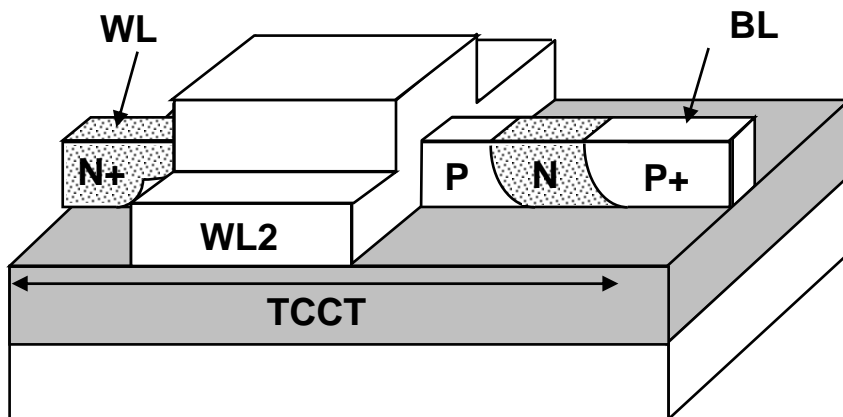
T-RAM Array Layout



Thyristor-RAM Future Outlook

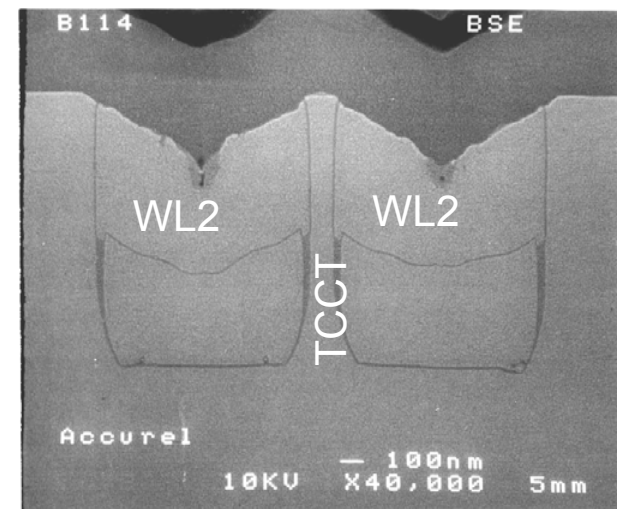
- Planar CMOS Roadmap Beyond 22nm is Uncertain
- Thyristor-RAM has Good Synergy w/ Frontrunner Alternatives
 - Such as MUGFET/FinFET, or UTB SOI Technologies
 - Improve Cell Characteristics due to Enhanced WL2 Coupling
- Ultra High Density RAM w/ Vertical Shallow Trench Thyristor

MUGFET / FinFET Thyristor-DRAM



UHD Trench Thyristor in Bulk

80nm Research Prototype





Summary

- ☉ Need for Larger On-chip RAM Growing
 - ☒ While 6T-SRAM Facing Scaling Challenges

- ☉ Thyristor-RAM Technology Offers:
 - ☒ Better Density-Performance than 6T-SRAM
 - ☒ Better Cost & Performance than eDRAM
 - ☒ Good Scalability

- ☉ Thyristor-RAM is Silicon Proven



Acknowledgements

- ❖ My Colleagues at T-RAM Semiconductor: B. Bateman, R. Chopra, V. Gopalakrishnan, R. Gupta, S. Nakib, S. Robins, R. Roy, M. Tarabbia, K.J. Yang
- ❖ H.J. Cho and Prof. J.D. Plummer
- ❖ Foundry Services Organization, Freescale Semi.