

EE Times:

## Chip makers, researchers dish on hottest chips, interconnects

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The Hot Chips and companion Hot Interconnects conferences provide a peek inside the leading multicore processors as well as research into the on- and off-chip networks that those future microprocessors may use.

[Hot Chips](#), Aug. 19-21 at Stanford University, provides an in-depth look into existing multicore CPUs such as IBM's Power6 and the latest graphics processors from Advanced Micro Devices and NVidia. In a rare new disclosure, startup Tileria Corp., founded by MIT professor Anant Agarwal, is expected to unveil its multicore [processor](#) for embedded systems.

IBM will deliver three papers on Power6, providing insight into how it has achieved power efficiency in the [dual-core](#) processor while still pushing the [edge](#) in [clock](#) speed. "This is notoriously difficult to achieve. Intel, for example, has largely stopped trying," said Rajeevan Amirtharajah, co-chair of the Hot Chips program committee and a professor at the University of California, Davis.

Among the papers Intel will present is one on power management techniques used in its upcoming 45-nm Penryn processor. AMD will detail Griffin, its first [CPU](#) for notebook computers. Sun Microsystems will describe Victoria Falls, a [cache](#) coherent version of its Niagara2, aimed at multsocket servers. And IBM will present its work on its next-generation [mainframe](#) processor.

T-RAM Semiconductor will present a paper on thyristor RAM. The device is seen as an embedded [memory](#) enabler for multicore processors because it can deliver DRAM-like densities at SRAM-like speeds.

"You can change the way you do things--like graphics rendering on die-- because of the amount of inexpensive RAM you can put on a chip, and you wind up managing L3 and L2 [chip](#) caches like paged memory," said John Sell, this year's Hot Chips chairman and a senior engineer in Microsoft's Xbox group.

A handful of papers will address embedded processors, including one from Texas Instruments on a DaVinci chip that can handle 30 frames/second of 720-progressive MPEG-4 video encoding at 400 mW.

A session dedicated to wireless will include papers on the 60-GHz radio work at startup SiBeam and an [802.11n](#) chip from Broadcom.

[Hot Interconnects](#), Aug. 22-24, will look further into the future at technologies such as on-chip networking, which is expected to be strategic in how microprocessors from AMD, IBM, Intel and others will compete.

"It's a new area of research. You can see a lot of techniques from supercomputers being used in multicore processors," said Fabrizio Petrini, co-chair of the conference and a researcher at IBM's T.J. Watson Research Center.

Researchers at Pennsylvania State University will describe an on-chip router that boosts chip performance as much as 30 percent while keeping power consumption and latency low. A paper from the University of Maryland will detail simulations of on-chip networks based on mesh-of-trees architecture connecting memory and processor units using various arbitration schemes.

Researchers at Columbia University will detail simulations of a hybrid electronic/photonics on-chip network.

But perhaps the most radical new idea will be Ethane, a new approach to business networking developed by Stanford University researchers. Ethane aims to make networks simpler to manage and secure by authenticating and identifying every source of traffic on the net.

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