

EE Times:

Stanford confabs explore multi-core CPUs, nets

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SAN JOSE, Calif. — The Hot Chips conference has posted [its program](#) that will provide a look inside some of today's leading multi-core processors in August at Stanford University. The companion Hot Interconnects event also has laid out [its agenda](#) for exploring research in the on- and off-chip networks tomorrow's processors someday may use.

This year's Hot Chips papers generally provide deeper looks into existing multi-core CPUs such as the IBM Power6 and the latest graphics processors from the Advanced Micro Devices and NVidia. In a rare new disclosure, startup Tiler Corp., founded by MIT professor Anant Agarwal, is expected to publicly unveil its multi-core [processor](#) for embedded systems.

IBM will deliver three papers on Power6, providing some insights on how it has achieved power efficiency in the [dual-core](#) processor while still pushing the edge in [clock](#) speed. "This is notoriously difficult to achieve. Intel, for example, has largely stopped trying," said Rajeevan Amirtharajah, co-chair of the Hot Chips program committee and a professor at the University of California, Davis.

Among other papers, Intel will describe power management techniques used in its upcoming 45nm [Penryn](#) processor family. AMD will detail [Griffin](#), its first [CPU](#) for notebook computers. Sun Microsystems will describe Victoria Falls, a [cache](#) coherent version of its Niagara2, aimed at multi-socket servers. And IBM will describe work on its next-generation [mainframe](#) processor.

[T-Ram Semiconductor](#) will describe its Thyristor RAM. The device is seen as an embedded [memory](#) enabler for multi-core processors because it can deliver DRAM-like densities at SRAM-like speeds.

"You can change the way you do things—like graphics rendering on die-- because of the amount of inexpensive RAM you can put on a chip, and you wind up managing L3 and L2 [chip](#) caches like paged memory," said John Sell, this year's Hot Chips chairman and a senior engineer in Microsoft's Xbox group.

A handful of papers will discuss embedded processors including one from Texas Instruments on a member of its DaVinci family launched earlier this year. The chip can handle 30 frames/second of 720-progressive MPEG-4 video encoding at 400mW.

One session is dedicated to wireless. It will include papers on the 60 [GHz](#) radio work at startup [SiBeam](#) and an 802.11n chip from Broadcom.

Hot Interconnects will look deeper into the future with a slate of papers that include several on new ideas for on-chip networking. Such interconnects are expected to be strategic for how microprocessors from companies such as AMD, IBM, Intel and others compete in the future.

"It's a new area of research. You can see a lot of techniques from supercomputers being used in multi-core processors," said Fabrizio Petrini, co-chair of the conference and a research at IBM's T.J. Watson R&D center.

Researchers at Pennsylvania State University will describe an on-chip router that boosts chip performance as much as 30 percent while keeping power consumption and latency low. A paper from the University of Maryland will detail simulations of on-chip networks based on a relatively new mesh-of-trees architecture connecting memory and processor units using a

variety of arbitration schemes.

Taking an even bigger leap forward, researchers at Columbia University will detail simulations of a hybrid electronic/photonic on-chip network. Their work focused on reducing the latency associated with setting up photonic paths and exploring a new direct memory access model.

Perhaps the most radical new idea at Hot Interconnects is [Ethane](#), a new approach to business networking developed by researchers at Stanford. The technique aims to make networks simpler to manage and secure by authenticating and identifying every source of traffic on the net. Ethane requires both a new set of switches using flow-control tables and controllers that decide whether or not to let traffic on the net based on a new policy language.

Other papers explore issues in data center networking at 10 bits/second. Academics from multiple labs in Virginia will show advantages in balancing the load of network traffic across multi-core CPUs using the iWARP protocol for offloading TCP processing. A group from Ohio State University will give an independent performance evaluation of the ConnectX architecture from Infiniband specialist Mellanox Technologies when used in multi-core CPUs.

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