Reliability of Thyristor-based Memory Cells

Craig Salling, Kevin J. Yang, Rajesh Gupta, Dennis Hayes,
Janice Tamayo, Vasudevan Gopalakrishnan, Scott Robins
T-RAM Semiconductor, Inc.
620 North McCarthy Blvd
Milpitas, CA 95035 USA
(408)-597-3661, craig@t-ram.com

***Abstract*—This is the first published study of the reliability of Thyristor-based high-speed memories. The T-RAM (Thyristor-based Random Access Memory) was characterized using test structures and multi-megabit product die fabricated in a 130nm SOI logic technology. The reliability lifetime of a nominal bit was investigated by subjecting TCCT devices (Thin Capacitively Coupled Thyristor) to a DC current stress. The resulting acceleration model yields a lifetime of 1.0E+40 yrs for the Data-1 state and 1.0E+5 yrs for the Data-0 state. These long lifetimes are consistent with the 26 FIT long-term failure rate found for 9 Mb arrays, from dynamic lifetest on 9Mb & 18Mb T-RAM product die having full SRAM functionality. The susceptibility of T-RAM arrays to soft errors was assessed by accelerated neutron testing, and accelerated alpha testing, of 9Mb T-RAM product die as well as 9Mb SRAM product die from three suppliers. n-SER for the T-RAM is 610 FIT/Mb, better than the average of 700 FIT/Mb for 6T SRAM technology. Exposure of the T-RAM product die to X-rays showed that they tolerate doses of 450 rad or more (3-4x the dose for X-ray inspections) without degradation of nominal TCCT retention times, and without functional failure of memory cells. Taken together, the results of this study shows that T-RAM is a reliable memory technology.**

Keywords-Thyristor, TCCT, T-RAM, SRAM, DRAM, memory technology

I. INTRODUCTION

T-RAM Semiconductor's breakthrough Thyristor-RAM technology (Fig. 1-2) is a novel memory technology that addresses both the memory wall problem and the memory scalability crisis. Thyristor-RAM technology is a Negative Differential Resistance based (NDR-based) RAM cell, called TCCT (Fig.3), which differentiates it from the traditional FET-based memory technologies such as 6T-SRAM and eDRAM. The result is a high-performance, high-density, and highly scalable embedded and discrete memory solution that allows for levels of memory integration not possible before. Unlike several other proposed embedded memory alternatives to 6T-SRAM, T-RAM Semiconductor has successfully developed the Thyristor-RAM technology from concept to production-readiness. Our Thyristor-RAM technology has been implemented on both Bulk and SOI CMOS, and it has been developed to demonstrate both SRAM [1] and DRAM [2] memories.

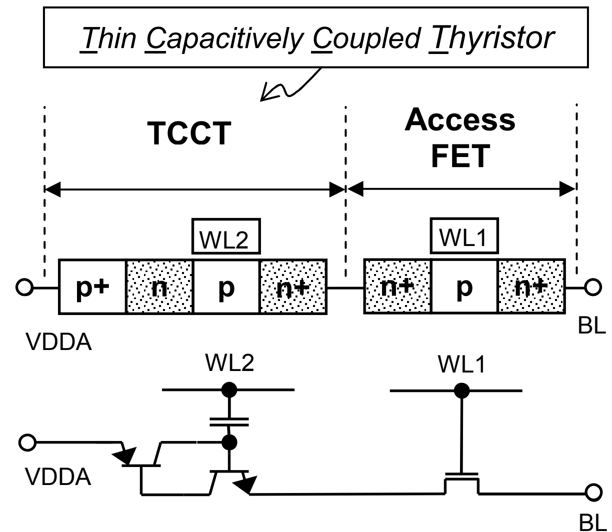


Figure 1. T-RAM SRAM cell basic structure and equivalent circuit model. TCCT consists of a pair of PNP and NPN transistors providing bi-stable characteristics and a WL2 gate providing capacitive coupling to the base of NPN device for high-speed switching of TCCT during write operation.

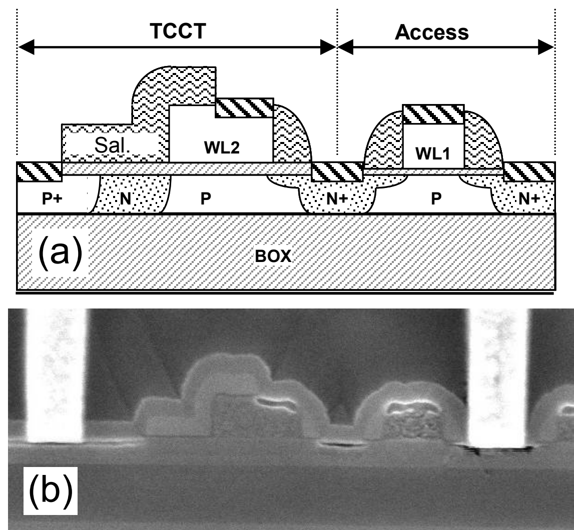


Figure 2. Cross-sectional view of the 130nm SOI SRAM-type T-RAM cell, shown as (a) schematic illustration and (b) TEM image. The cell is integrated into a baseline logic process using only additional masks/implants.

The present paper will assess the reliability of the SRAM-type cell (Fig.1), built in a 130nm SOI logic technology (Fig.2). The T-RAM invention uses capacitive coupling of a gate (WL2) to the base of the constituent NPN transistor to achieve high-speed switching of the TCCT during write operation. The read current margin between the on-state, Data-1, and off-state, Data-0, of the TCCT (Fig.3) is guaranteed by device design to be at least 6 orders of magnitude (Fig. 4).

II. TCCT Test Structures

We investigated the reliability of the read margin for the T-RAM cell by using accelerated testing of TCCT test structures to characterize the long-term behavior I_{off} (for Data-0) and I_{on} (for Data-1). Degradation of the on-state and off-state currents was accelerated using a DC anode-cathode current, I_{stress} , through the TCCT that was several times larger than the current I_{use} that flows during normal operation of the T-RAM cell. We developed an empirical acceleration model for the time-to-fail, and estimated the lifetime of a nominal bit with respect to the TCCT of that bit continuing to have a negligible read current for the Data-0 state and a large read current for the Data-1 state. We defined a read margin failure as the point when I_{off} had increased 20% above its initial value, or I_{on} had decreased 20% below its initial value.

A. Characterization

Early experiments showed that a DC on-state current through a forward-based TCCT is an effective stress for reliability studies. In operation of a T-RAM array, DC current flows only briefly through the TCCT, during read, write, or refresh of the Data-1 state. High-frequency testing on TCCT test structures, up to 125 MHz, showed that no additional degradation was induced by switching the TCCT between a Data-0 (off) and Data-1 (on) state, nor by repeated Read or Write in an unchanging data state. Thus, a DC current stress was used in the present paper to characterize TCCT degradation and estimate the nominal lifetime of the TCCT.

Figure 4 shows the average on-state and off-state current per TCCT device as a function of stress time, for various levels of applied stress voltage. Testing was done with the TCCT anode biased positive to V_{anode} and the cathode held at 0V. TCCT current was measured out of the cathode. During the DC current stress, the TCCT was in the on-state with V_{anode} set to V_{stress} and the WL2 gate electrode set to 1.5V. V_{stress} values ranged from 1.3V to 2.5V. The range of V_{stress} values used for characterizing I_{off} and I_{on} were chosen to give readily detectable degradation within 10,000 sec without causing overstress of the TCCT (e.g. WL2 oxide breakdown). During the measurement of I_{on} and I_{off} , V_{anode} was set to $V_{measure}$, WL2 was held at -1.6V, and I_{TCCT} was measured as the current out of the cathode. To simulate the TCCT biasing (Fig. 3) during Read of a T-RAM cell, $V_{measure}$ = 1.1V was used for I_{on} and $V_{measure}$ = 1.9V was used for I_{off}. The WL2 gate current is also measured, along with the current into the anode.

For the set of devices tested, the average I_{off} and I_{on} exhibit a peak (Fig. 4) as stress time is increased. These peaks suggest that the degradation of the current is self-limiting.

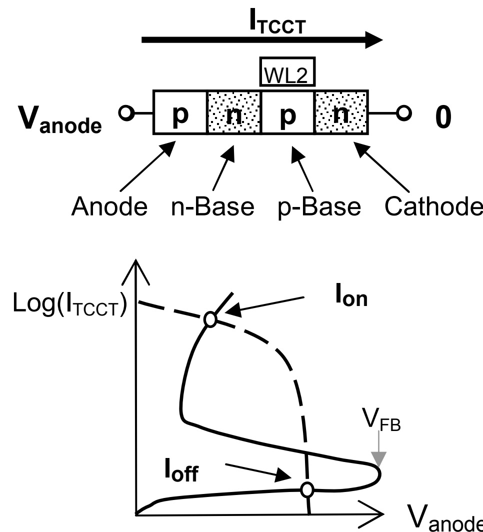


Figure 3. Illustration of the TCCT during characterization, and the load-line diagram of the T-RAM cell during Read operation. The TCCT on-state current, I_{on} , defines the Data-1 state and its off-state current, I_{off} , defines Data-0 state.

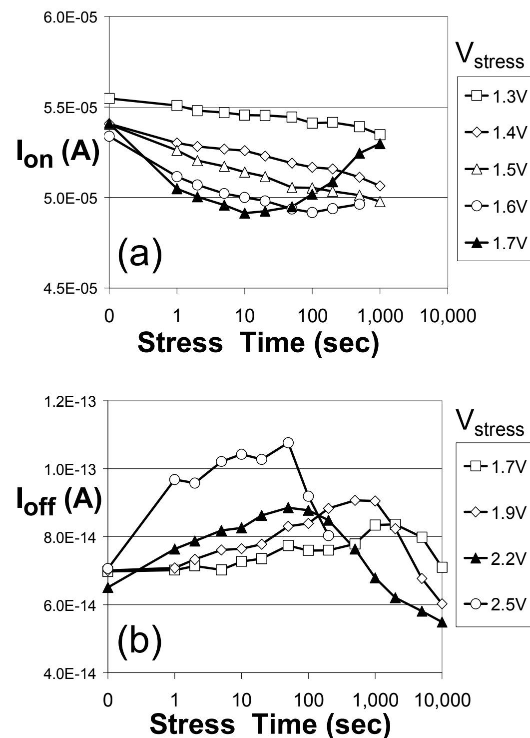


Figure 4. Average TCCT (a) I_{on} and (b) I_{off} as a function of stress time and stress voltage. I_{on} measured for a single TCCT at 32°C. I_{off} is the average current per TCCT of a 56-device array tested at 105°C. I_{on} and I_{off} degrade until a stress time t_{peak} is reached, and afterwards improve.

However, the peaks could be artifacts, caused by (a) slowly-varying offset in the current measurement, or (b) increased leakage of the WL2 oxide. We characterized the current measurement itself by doing the stress-test on fresh die with zero stress voltage. The resulting I_{on} and I_{off} statistics yielded the long-term drift (systematic error) and short-term noise (random error) in our current measurements. There is a long-term drift of approximately 2E-15 A during the course of any given degradation test, and short-term noise of 1E-15 A. The amplitude of the peak in the TCCT current (Fig. 4) was 5.0E-6 A for I_{on} and 3E-14 A for I_{off}, over 10x larger than the background drift and noise in the current measurement. Thus, the observed peak in TCCT current cannot be explained by drift or noise inherent to the current measurement process.

Since the TCCT current is measured at the cathode, an increase in leakage current from the p-base of the TCCT to the negatively-biased WL2 would cause a reduction in the measured TCCT current. The measured WL2 gate currents are insignificant compared with the change in I_{off} (or I_{on}) observed during the stress test, and show negligible change compared to the TCCT current (Fig. 5). Thus, the decline in I_{off} after the peak is not due to increased WL2 oxide leakage shunting current away from the TCCT cathode. We conclude that the peaks exhibited by I_{on} and I_{off} in Fig. 4 indicate the degradation of the TCCT read margin is in fact self-limiting.

B. Acceleration Model

In order to estimate the nominal lifetime of the TCCT, an acceleration model was determined for t_{63} , the time at which 63% of the TCCT devices fail. The general form of the model is

$$t_{63} = g(I_{stress}) * h(T) \quad (1)$$

where I_{stress} is the DC current that flows through the TCCT and T is the junction temperature of the TCCT. The form of the model assumes negligible interaction between the current and temperature variables. Estimates of the heat flow from the TCCT to the wafer chuck indicates that self-heating is an insignificant perturbation. In addition, the measured on-state current at a fixed anode-cathode voltage, is a weak function of temperature.

t_{63} as a function of stress current and temperature is obtained from the failure statistics for a collection of individual test structures. The I_{on} and I_{off} data of individual test structures were measured as a function of stress time, t_{stress} , and used to calculate the degradation parameter

$$Y_j(t_{stress}) = [\, I_j(t_{stress}) - I_j(0) \,] \,/\, I_j(0) \quad (2)$$

where Y_j is the fractional change in current for the jth test structure, and I_j is I_{on} or I_{off} for that test structure. At early times, $1\text{sec} \le t_{stress} < t_{peak}$, the degradation of individual test structures is best described (Fig. 6) by a logarithmic model

$$Y_j(t_{stress}) = a_j + b_j * \text{LOG}(t_{stress}) \quad (3)$$

where $a_j < 0$, $b_j < 0$ for degradation of the on-state current, and $a_j > 0$, $b_j > 0$ for degradation of the off-state current. The time to failure, t_{fail} , is defined as the time for Y_j to reach - 0.20 for I_{on} or + 0.20 for I_{off}.

The Weibull distribution fits the t_{fail} values well for both I_{off} (Fig. 7a) and I_{on} (Fig. 7b) and yields values for t_{63} as a function of stress current. The current acceleration of t_{63} closely follows (Fig. 7c) a power-law model

$$t_{63} = t_{63_use} * (I_{stress} / I_{use})^{-n} \quad (4)$$

where t_{63} is the value at I_{stress} , t_{63_use} is the value at I_{use} = 35 uA, n = 8.8 for I_{off} , and n = 27.2 for I_{on} .

Additional measurements were done to determine the thermal acceleration of the TCCT. Degradation was characterized as a function of temperature, at fixed stress voltage (1.9V for I_{off} , 1.7V for I_{on}). Failure was again defined as a 20% increase in I_{off} or a 20% decrease in I_{on}.

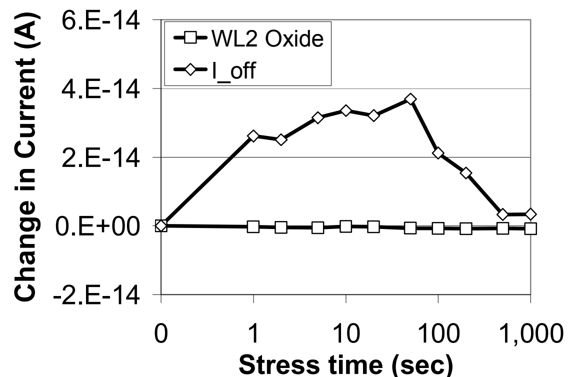


Figure 5. The change in current during a 2.5V stress for an average TCCT's WL2 oxide leakage, compared to its off-state current. The decline in measured I_{off} at long stress times is not due to an increase in WL2 leakage. This, plus the negligible measurement error, indicates that the peaks seen in Fig. 4 are genuine, and degradation of I_{off} and I_{on} are self-limiting.

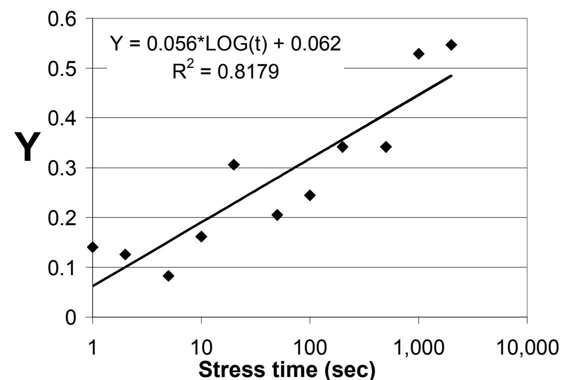


Figure 6. The fractional change, Y, in Ioff as a function of stress time, for Vstress = 1.7V and T=105C. The failure time, tfail, defined by Y = +0.20, occurs at approximately 10 sec for this test structure.

The time-to-fail statistics were well fit by the Weibull distribution, yielding values of t_{63} as a function of temperature. These data closely follow (Fig. 8) an Arrhenius model

$$t_{63} = A * \mathrm{EXP}(E_a/kT) \quad (5)$$

where A is an empirical pre-factor, E_a is the activation energy, k is Boltzmann constant, and T is the silicon junction temperature in Kelvin. This analysis yields an activation energy of 0.54 eV for I_{off} degradation and -0.92 eV for I_{on} degradation.

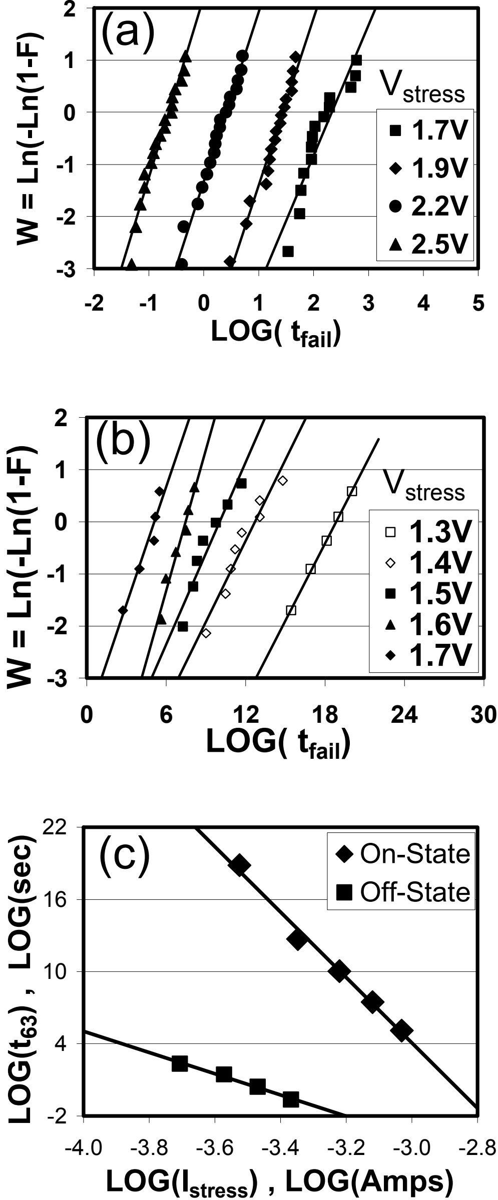


Figure 7. Weibull plots of the t_{fail} distributions for (a) I_{off} and (b) I_{on} as a function of stress voltage. These plots yield t_{63} as a function of stress current, I_{stress} . The current acceleration for t63 follows a power law model (c).

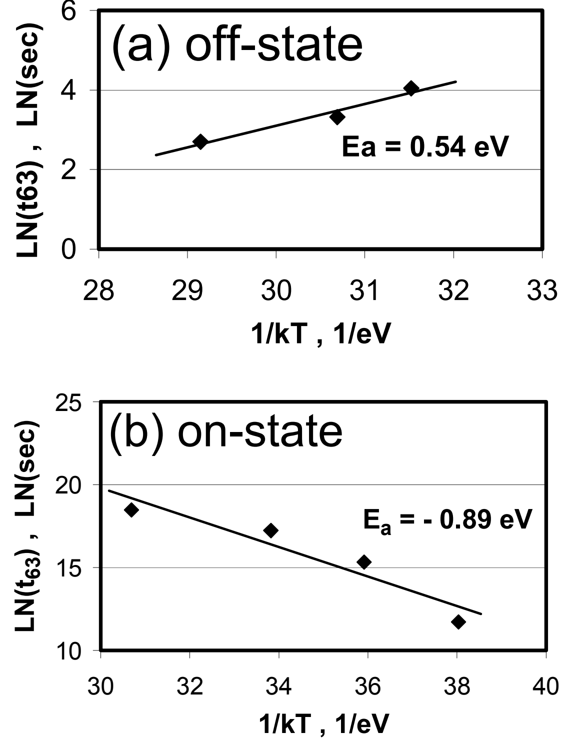


Figure 8. Thermal acceleration model for the TCCT. The Arrhenius model fits the t_{63} data for degradation of (a) off-state and (b) on-state current.

C. TCCT Degradation Mechanisms

These activation energies enable us to understand the mechanisms responsible for degradation of I_{off} and I_{off}. When the TCCT is the off-state, the junction between the n-Base and the p-Base (Fig. 3) is reverse-biased, and this is underlying cause of the miniscule current flow, I_{off}, from Anode to Cathode. The leakage current, I_{np}, of the reverse-biased n-Base/p-Base junction provides a base current for the constituent npn transistor formed by the n-Base, p-Base, and Cathode. I_{off} flowing out of the Cathode can be approximated as this base current plus the collector-emitter current it causes to flow in the npn bipolar. Thus, we have the expression

$$I_{off} \sim I_{np} * (1 + \beta_{npn}) \quad (6)$$

where β_{npn} is the gain of the constituent npn transistor. As silicon defects are introduced by the action of I_{TCCT} during stress, I_{np} will increase due to increased generation-recombination from defects created in the n-Base/p-Base junction. This degradation mechanism causes I_{off} to increase with stress, which is what is observed to be the case for stress times $t < t_{peak}$. The activation energy for the increasing I_{off} is found to be 0.54 eV, in reasonable agreement with the value 0.6 eV observed for soft breakdown of reverse-biased *pn* junctions [3]. Thus the activation energy supports the hypothesis that I_{off} degradation is caused by stress-induced

defects in the n-Base/p-Base junction, which result in increased I_{np}.

Experiments with test structures comprising just the constituent npn transistor of the TCCT verify that I_{TCCT} causes a long-term reduction of β_{npn} . A likely mechanism for this reduction is the creation of defects in the p-Base region, decreasing β_{npn} . Thus, effect of stress current on the npn transistor causes I_{off} to decrease. Thus, the observed peak in I_{off} with stress time could be explained by degradation of I_{np} followed by a slower degradation of β_{npn} becoming dominant at longer stress times.

When the TCCT is in the on-state, n-Base and p-Base regions become a single intrinsic region having a high carrier concentration, due to high-level injection from the Anode and Cathode. Thus, the TCCT in the on-state acts as a *p-i-n* diode. The carrier concentration in the intrinsic region determines its resistance, and this resistance limits the on-state I_{TCCT} to its observed value I_{on}. In the optimized design of the TCCT, the Anode/n-Base junction has a shorter recombination lifetime, and provide less injection into the intrinsic region, than the p-Base/Cathode junction. This leads to a lower steady-state carrier concentration for the end of the intrinsic region that is near the Anode/n-Base junction. The total resistance of the intrinsic region is set by this lower-concentration end, and hence is set by the lifetime of the Anode/n-Base junction.

Thus, a plausible mechanism for stress-induced reduction of Ion is that the stress current creates defects in the Anode/n-Base junction, reducing its recombination lifetime and injection efficiency. This increases the total resistance of the intrinsic region and decreases I_{on} .

The recombination lifetime at the Anode/n-Base junction also affects its forward-biased current, I_{an} . One can measure I_{an} by placing the TCCT in the on-state and raising WL2 from the standard -1.6V bias to a + 1.5V bias. This has the effect of creating an inversion layer in the p-Base at the WL2 gate, thus shorting the n-Base to the Cathode. The result is to isolate the Anode/n-Base constituent diode of the TCCT device.

Thus, I_{an} degradation will show the same temperature dependence as the contribution of the Anode/n-Base junction lifetime to the degradation of I_{on} . The stress-test study was repeated at two temperatures (50°C and 70°C) for a set of TCCT devices, with the failure time defined as a 20% change in I_{an} . The failure statistics of individual devices followed a Weibull distribution, and yielded t63 values. These values allowed us to estimate an activation energy of -0.90 eV for degradation of the Anode/n-Base junction (Fig. 9) , in good agreement with the value of -0.89 eV observed for degradation of I_{on}. This supports the hypothesis that I_{on} degradation is due to stress-induced defects in the Anode/n-Base junction causing a reduction in the overall carrier concentration in the intrinsic region (n-Base/p-Base) of the TCCT in the on-state.

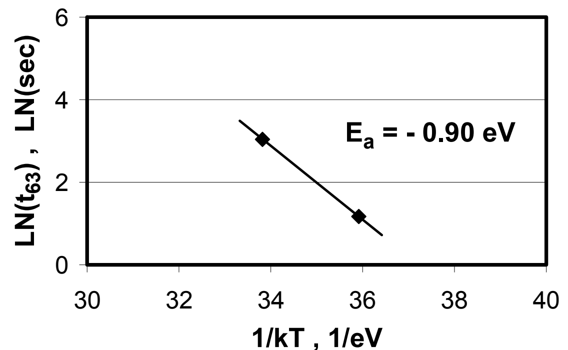


Figure 9. Thermal acceleration model for degradation of the forward-biased Anode/n-Base junction of the TCCT. The degradation of this junction causes the degradation of I_{on}, and explains the negative activation energy observed for I_{on} degradation.

D. *TCCT Nominal Lifetime*

In use, as part of a T-RAM memory array, the TCCT's on-state current stress is not constant, but has an estimated worst-case duty cycle δ = 1.0E-3. With this information, the current acceleration model can be used to estimate the lifetime of a nominal bit with respect to read margin of the TCCT on and off states. The resulting nominal lifetime is 1.0E4 yrs for the Data-0 state at 105°C, and 1.0E+39 yrs for the Data-1 state at 32°C. Using the thermal acceleration model, these translate to nominal lifetimes of 1.0E+5 yr for Data-0 read margin and 1.0E+40 yrs for Data-1 read margin at the standard junction temperature of 55°C during use.

Thus, the read-margin reliability of the TCCT is dominated by the off-state, since this has a considerably shorter nominal lifetime. This fact informed our estimate of a FIT rate for the T-RAM memory from lifetest data on 9Mb and 18Mb die. We use an activation energy of 0.6 eV, because it is the conventional choice for silicon integrated circuits, and because it reflects the greater importance of off-state degradation (0.55 eV) than on-state degradation (-0.92 eV) to potential failure of bits in T-RAM products.

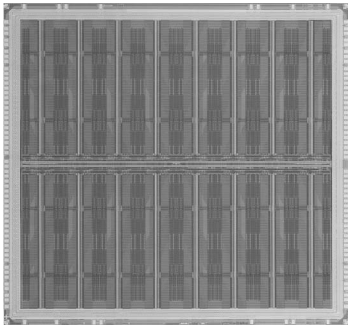
III. 9MB & 18MB T-RAM PRODUCT DIE

The reliability of the T-RAM cell was also assessed using 9Mb and 18Mb product die, built using the same 130nm SOI logic technology that was used to fabricate the test structures. Both the 9Mb and 18Mb die have full SRAM functionality. The 9Mb chip demonstrates a fully-functional multi-megabit T-RAM memory. The 18Mb chip demonstrates the manufacturability and commercial viability of the T-RAM technology. It has the capacity for redundancy to improve yield and product reliability, and built-in test modes to expedite manufacturing screens. It also uses an improved design for the sense amp and other circuit blocks, based on characterization of the 9Mb test chip.

A. Testing

Only units that passed the manufacturing test flow were used in reliability assessments. This flow consists of guardbanded tests at cold and hot at wafer sort and again after a 48hrs 125°C voltage-accelerated Burn-In. All manufacturing testing was done in-house using Advantest T5581P Memory Tester, with an prober for testing wafers, and an 8-socket test head for testing packaged units. The standard test program included standard pin continuity tests, junction temperature measurements, and a full set of test patterns to capture all potential failure mechanisms of the array. The guardband and burn-in conditions were developed from extensive early HTOL studies that included repeated testing at HTOL readpoints to verify that guardbanded tests in manufacturing catch all bits that fail subsequently at use conditions. The resulting test flow also achieved competitive yields at wafer sort, final (packaged) test, and after 48 hrs. Burn-in.

For the reliability studies, the guardbanded testing after Burn-in provided the pre-stress testing, using the full suite of patterns. The post-stress testing was done at nominal use conditions. For all studies, the post-stress testing was also done using the high-speed memory test system. The only exception is the neutron SER testing, which used a mobile system constructed by iROC Corp.



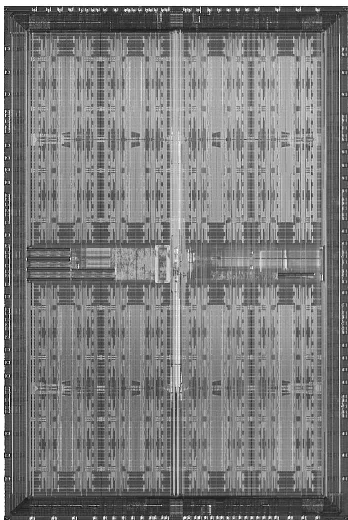


Figure 10. 9Mb (top) and 18Mb (bottom) T-RAM product die having full SRAM functionality.

B. Lifetest

Lifetest at 125°C was performed on 9Mb (300 units, 1000hrs) and 18Mb (200 units, 1000hrs) T-RAM product die taken from 6 manufacturing lots. Extensive testing at 48, 168, 500, and 1000hrs readpoints showed no failures of the T-RAM cell for all known RAM failure mechanisms. The data may be combined to yield an EFR of 0.13% and LFR of 26 FIT for 9Mb arrays with 60% CL.

C. Soft Error Rate

The susceptibility of the T-RAM cell to Soft Errors was assessed for both cosmic-ray neutrons (n-SER) and proximal-source alpha particles (α-SER). Accelerated neutron testing was done using the wide-spectrum neutron beam at the LANSCE facility and a tester built by iROC Corp., which exercised the die with repeated read and write of alternating checkerboard and inverse checkerboard patterns. The units were in standby for a duration after each write to accumulate errors for the subsequent read. The measured n-SER failure rates of six 9Mb T-RAM memories are compared to those of six 9Mb 6T SRAM products from each of three suppliers. The T-RAM n-SER is 610 FIT/Mb, better than the average 700 FIT/Mb for available commercial 6T SRAMs.

Accelerated alpha particle testing was performed in-house by exposing de-capped units to the flux from a Thorium foil source while the units were tested with the high-speed memory test system. The Thorium foil had a flux F_stress, of 3.70E+05 α/cm2-hr, compared to the flux F_use, of 0.001 α/cm2-hr, expected for contemporary packaging material. The tester exercised the die with repeated read and write of alternating checkerboard and inverse checkerboard patterns. The units were in standby for a duration after each write to accumulate errors for the subsequent read. The measured α-SER failure rates of six 9Mb T-RAM memories are compared to those of six 9Mb 6T SRAM products from each of three suppliers. The SRAM products had α-SER values of 40, 100, 190, and 470 FIT/Mb. The T-RAM devices had an α-SER of 460 FIT/Mb, within the range of SRAM devices.

D. X-ray Exposure

Conventional DRAM memories fail when exposed to X-ray doses as low as 120 rad [4-5]. A DRAM cell is comprised of a capacitor connected to the source diffusion region of an access FET. The refresh frequency required by the cell, to maintain it's data state, is set by the leakage current of pn junction of the source region. X-rays induce defects in this junction, and hence increase leakage current and increase the refresh frequency required. As we have seen, the creation of defects in the pn junctions of the TCCT cause degradation of the T-RAM memory's Read margin. Thus, it is important to ascertain the sensitivity of T-RAM memories to X-ray dose.

We exposed 9Mb T-RAM product die to cumulative X-ray doses of 0, 150, 450, and 1000 rad. At each stress readpoint,

the units were tested for all known RAM failure mechanisms. The testing included functionality tests, as well as characterization of the distribution of Data-0 retention times for the cells of the T-RAM array (Fig.9a). The shorter retention times at 0 rad is due to the guardband between pre-stress and post-stress testing, and is also seen in the control group (no X-ray dose), as shown in Fig. 9b. No statistically-significant shift of the main distributions occurred at any dose, and no failures occurred at 450 rad or below. Three units, out of the 15-unit sample, failed for a few bits at 1000 rad. Thus, the T-RAM technology is much more robust with respect to X-ray exposure than conventional DRAM memories.

IV. CONCLUSIONS

The characterization of TCCT test structures yield a nominal lifetime of 1.0E+5 yr for the Data-0 read margin and 1.0E+40 yrs for Data-1 read margin at standard use conditions. Table I summarizes the reliability results for T-RAM product die. These results show reliability comparable to commercial SRAM products. Taken together, the results of this study show that T-RAM is a reliable and manufacturable memory technology.

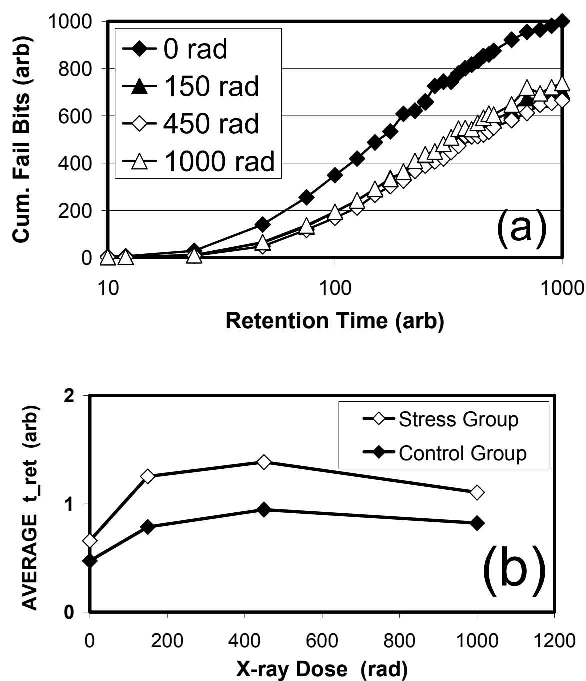


Figure 11. Effect of X-rays on the (a) Data-0 retention time distribution and (b) t_{ret} point on distribution where cumulative fail bits is 200, in arbitrary units.

TABLE I. SUMMARY FOR 9MB T-RAM ARRAYS

Metric	Stress	Failures	Conclusion
EFR	168hrs lifetest at 125C on 9Mb and 18 Mb units	0/702 9Mb arrays	0.13% @ 60%CL
LFR	1000hrs lifetest at 125C on 9Mb and 18Mb units	0/702 9Mb arrays	26 FIT @ 60% CL
n-SER	1.0E+09 n/cm2 neutron fluence on 9Mb units	400 bits/unit 6 units	610 FIT/Mb @ 60% CL
α-SER	4.5E+04 α/cm2 alpha fluence on 9Mb units	100 bits/unit 6 units	460 FIT/Mb @ 60% CL
X-ray max. passing dose	Inspection tool doses of 0, 150, 450, 1000 rad on 9Mb units	0/15 units at 450 rad	450-1000 rad
		3/15 units at 1000 rad	

ACKNOWLEDGMENT

The authors wish to thank Ram Gooty and John Joseph for developing the test programs used in the studies of the product die, Pradeep John for facilitating die assembly and n-SER data collection, Shridevi Guuram and Tracy Li for developing the programs used for automated data analysis, Marc Tarrabia for process engineering support and help with the X-rays study, and Rajesh Chopra for insightful help understanding circuit operation on the product die.

REFERENCES

[1] F. Nemati, et. al., "Fully Planar 0.562µm2 T-RAM cell in a 130nm SOI CMOS logic technology for high-density high-performance SRAMs," *International Electron Devices Meeting Tech. Dig.*, 2004, pp. 274-278.

[2] H. Cho, et. al., "A novel capacitor-less DRAM cell using thin capacitively-coupled Thristor (TCCT)," *International Electron Devices Meeting Tech. Dig.*, 2005, pp. 321-324

[3] Schnable, G. and Keen, R., *IEEE International Reliability Physics Symposium Proc.*, 1969, p. 170.

[4] A. Ditali, M. Ma, B. Black, S. Wen , and S. Chung, "Kinetic analysis of X-ray irradiation induced static refresh failure mechanism in DRAM," *IEEE International Reliability Physics Symposium Proc.*, 2007, pp. 71-77.

[5] A. Ditali, M. Ma, and M. Johnston, "X-ray radiation effect in DRAM retention time," *IEEE Trans. Device and Materials Reliability*, vol 7, no. 1, 2007, pp. 105-111.